

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800
Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 3/5/04 Serial # 09/914,077 Priority Application Date _____
Your Name M. Lewis Examiner # _____
AU 2892 Phone 272-1838 Room 5A30
In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

03-05-04 203:59 IN

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ☒ Nonpatent Literature _____ Other _____
Secondary Refs ☒ Foreign Patents _____
Teaching Refs ☒ _____

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-6, 28 & 29

Problem see pages 1-3

Solution: " " 3-10

Staff Use Only
Searcher: Speckhard
Searcher Phone: _____
Searcher Location: STIC-EIC2800, CP4-9C18
Date Searcher Picked Up: 3/10/04
Date Completed: 3/4/04
Searcher Prep/Rev Time: 180
Online Time: 140

Type of Search
Structure (#) _____
Bibliographic ☒
Litigation _____
Fulltext _____
Patent Family ☒
Other all

Vendors
STN ☒
Dialog ☒
Questel/Orbit _____
Lexis-Nexis _____
WWW/Internet _____
Other _____



STIC Search Report

EIC 2800

STIC Database Tracking Number: 116165

TO: Monica Lewis
Location: JEF 5A30
Art Unit : 2822
Friday, March 12, 2004

Case Serial Number: 09/914077

From: Irina Speckhard
Location: EIC 2800 JEF 4B59
Phone: (571) 272-2554
irina.speckhard@uspto.gov

Search Notes

Examiner Lewis,

Please find attached first-pass prior-art search results from the patent and non-patent abstract databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard



03/11/2004

09/914,077

11mar04 14:48:10 User267149 Session D1284.1

File 342:Derwent Patents Citation Indx 1978-04/200414

(c) 2004 Thomson Derwent

S1 6 PN=(US 6176010 OR US 6049461 OR US 5852289 OR US 4960983
OR US 5339847 OR US 5598032)

? MAP PN/CT=

? MAP PN/CG=

SYSTEM:OS - DIALOG OneSearch

File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)

(c) 2004 JPO & JAPIO

*File 347: JAPIO data problems with year 2000 records are now fixed.

Alerts have been run. See HELP NEWS 347 for details.

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200416

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Set	Items	Description
S1	218	S1:S44
S2	129	S1 AND ((INTEGRAT?(3N)(CIRCUIT? OR LOOP? ?)) OR IC OR CHIP? ?)
S3	113	S2 AND ((INTEGRAT?()CIRCUIT? OR IC)(3N)ELEMENT? ? OR CARD? ?)
S4	0	S3 AND (COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE??- ??)(3N)COMPOSIT?
S5	0	S3 AND (COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE??- ??)(3N)(DIAMETER? OR WIDE??? OR WIDTH)
S6	3	S3 AND (RECTANGULAR? OR SQUARE??? OR ANGLE??? OR PERPENDIC- ULAR?)(3N)(COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE??- ??)
S7	110	S3 NOT S6
S8	4	S7 AND (CONTACTLESS OR WIRELESS)(3N)COMMUNICAT??????
S9	106	S7 NOT S8
S10	1	S9 AND (EXTERNAL???????? OR OUTSIDE)(3N)EQUIPMENT
S11	105	S9 NOT S10
S12	6	S11 AND CONDUCT??????(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYE- R???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S13	99	S11 NOT S12
S14	0	S13 AND (ELECTROLESS(2N)(PLATING OR PLATE??? OR COVER? OR - COAT?) OR ELECTROPLAT????? OR ELECTRO()(PLATING OR PLATE??? OR COVER? OR COAT?) OR ELECTROFORM???????? OR ELECTROFORM??????)
S15	3	S13 AND (ALUMINUM OR AL OR NICKEL OR NI OR COPPER OR CU OR CHROMIUM OR CR)
S16	96	S13 NOT S15
S17	4	S16 AND ELECTRIC????????(3N)(INSULAT? OR DIELECTR?)

6/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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04478397

IC CARD AND MANUFACTURE THEREOF

PUB. NO.: 06-122297 [JP 6122297 A]
PUBLISHED: May 06, 1994 (19940506)
INVENTOR(s): SUZUKI HIROSHI
HISHINUMA HIROYUKI
SAITO MASAO
OIKE HIDESHI
APPLICANT(s): SONY CHEM CORP [488106] (A Japanese Company or Corporation),
JP (Japan)
APPL. NO.: 05-034890 [JP 9334890]
FILED: January 29, 1993 (19930129)
JOURNAL: Section: M, Section No. 1649, Vol. 18, No. 413, Pg. 21,
August 03, 1994 (19940803)

ABSTRACT

PURPOSE: To manufacture an IC card having a specified uniform thickness with high productivity and improve connection reliability of a transmitting/ receiving coil to be provided in the IC card.
CONSTITUTION: As a transmitting/receiving coil 3a to be provided in an IC card, a coil having a straight angle line wound thereon is used. As a method for shaping into a card, electronic parts 3a and 3b are fixed on an insulating base material 1 and a spacer 4 is arranged on the outer periphery of the insulating base material. The inside surrounded by the spacer 4 is filled with a UV setting resin 5, on which a transparent film 6 or a transparent plate is laid. The UV setting resin 5 is set by UV irradiation.

6/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009805120

WPI Acc No: 1994-084975/199411

XRPX Acc No: N94-066525

IC card used for security transportation, communication - has transmission and reception coil around which rectangular wires are wound

Patent Assignee: SONY CHEM CORP (SONY)
Inventor: HISHINUMA H; OIKE H; SAITO M; SUZUKI H
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 587011	A1	19940316	EP 93113858	A	19930830	199411 B
JP 6122297	A	19940506	JP 9334890	A	19930129	199423
EP 587011	B1	19980729	EP 93113858	A	19930830	199834
DE 69319978	E	19980903	DE 619978	A	19930830	199841
			EP 93113858	A	19930830	

Priority Applications (No Type Date): JP 9334890 A 19930129; JP 92257510 A 19920831

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 587011	A1	E	12	G06K-007/08	

Designated States (Regional): DE FR GB
JP 6122297 A 5 B42D-015/10
EP 587011 B1 E G06K-007/08
Designated States (Regional): DE FR GB
DE 69319978 E G06K-007/08 Based on patent EP 587011

Abstract (Basic): EP 587011 A

The IC card has a coil around which rectangular wires are wound is used as a transmission and reception coil. Electronic parts are fixed on an insulating base material. A spacer is disposed on an outer peripheral portion of the material. An ultraviolet ray curing resin is filled into the base material at its inside surrounded by the spacer.

A transparent film of plate is disposed on the ultraviolet ray curing resin. the UV ray curing resin is radiated with rays so that the resin is cured.

ADVANTAGE - Card formed with predetermined uniform thickness.

Dwg.1g/9

6/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009263447

WPI Acc No: 1992-390858/199248

XRPX Acc No: N92-298102

Closed coupling for one and two coil inductive coupling for smart cards - receives card passed through gap in transformer core for card coil to couple inductively for transmission of power and signals without any contact

Patent Assignee: ANGEWANDTE DIGITAL ELEKTRONIK (ANGE-N)

Inventor: HASS W; KREFT H; MACKENTHUN H

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4115867	A	19921119	DE 4115867	A	19910515	199248 B
DE 4115867	C2	19941027	DE 4115867	A	19910515	199441

Priority Applications (No Type Date): DE 4115867 A 19910515

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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DE 4115867	A		5	G06K-007/01	
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DE 4115867	C2		5	G06K-007/01	
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Abstract (Basic): DE 4115867 A

A non contact system is used for read and write operations carried out on a 'smart' card, together with the supply of electrical power. The power and signal transmission is made using inductive coupling and uses two transformer units (1,2) with the card passing through a gap in the transformer core.

Each transformer has a winding and a field is generated that interacts with coils formed within the card. Typically the coil windings have a rectangular, spiral form.

ADVANTAGE - Non-contact signal and power transmission.

Dwg.1/4

Abstract (Equivalent): DE 4115867 C

Pot core arrangement in write/read stations for contactless energy and data transmission by electromagnetic oscillations to chip or I.C. cards, with one or two coils. The transducers or repeater

coils (1,2) are built from pot cores in such a way that the magnetic flux in the centre of the core flows through the faces and is enclosed by the windings of the card.

The outer edge of a core has cutouts (D) on at least one side, being enlarged when adjacent (C) and having a greater reluctance for the magnetic flux. These cutouts lie on the axis connecting the two coils of a card.

USE/ADVANTAGE - Credit or payment cards. Same structure can be used for one or two coils.

8/3,AB/1 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

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04989610

CONTACTLESS IC CARD INTERFACE DEVICE AND COMMUNICATION SYSTEM
USING THE SAME

PUB. NO.: 07-282210 [JP 7282210 A]

PUBLISHED: October 27, 1995 (19951027)

INVENTOR(s): TAKAHIRA KENICHI
HAYAMIZU KOICHI

APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or
Corporation), JP (Japan)

APPL. NO.: 06-070913 [JP 9470913]

FILED: April 08, 1994 (19940408)

ABSTRACT

PURPOSE: To access a mass-storage data memory fast by reading the contents of a contactless IC card in the memory of the interface device and accessing it.

CONSTITUTION: The contactless IC card interface device 11 is equipped with an interface controller 13 which controls two-way signals to and from an external host device, a communication controller 15 which controls a data communication with the contactless IC card corresponding to the output signal of the external host device, and a memory 14 whose data can be accessed from the interface controller 13 and communication controller 15. When data are read out of the contactless IC card, the communication controller 15 transfers the data from the contactless IC card to the memory 14 with the output signal of the host device. The host device can access the data, transferred to the memory 14, fast through the interface controller 13.

8/3,AB/2 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012785170

WPI Acc No: 1999-591396/199950

XRPX Acc No: N99-436173

Data carrier such as credit card with implanted metal lead frame
based module for contactless communication

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS AB (PHIG
); US PHILIPS CORP (PHIG)

Inventor: RIENER T; SCHMALLEGGER P

Number of Countries: 020 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9950792	A1	19991007	WO 99IB262	A	19990215	199950 B
EP 998725	A1	20000510	EP 99901849	A	19990215	200027
			WO 99IB262	A	19990215	
US 6321993	B1	20011127	US 99275370	A	19990324	200175
JP 2002500794	W	20020108	JP 99549077	A	19990215	200206
			WO 99IB262	A	19990215	

Priority Applications (No Type Date): EP 98890083 A 19980327

Patent Details:

Patent No	Kind	Lang	Pg	Main IPC	Filing Notes
WO 9950792	A1	E	16	G06K-019/077	
Designated States (National): JP					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 998725	A1	E		G06K-019/077	Based on patent WO 9950792
Designated States (Regional): AT DE FR GB NL					
US 6321993	B1			G06K-019/06	
JP 2002500794	W		14	G06K-019/077	Based on patent WO 9950792

Abstract (Basic): WO 9950792 A1

Abstract (Basic):

NOVELTY - A module (4) having contact configuration (5) and chip (6) is implanted in a recess (3). Two contacts of module are connected to chip contacts (50,51) and coil contacts (52,53) of transmission coil (54) in data carrier. The contact configuration made by metal lead frame, has coplanar sides (16,17) and central section (18), which are mechanically connected to chip cover (7).

DETAILED DESCRIPTION - The chip cover made of electrically insulating metal covers the module contacts and chip. The contact configuration is covered by an insulating layer (60) made of polyvinyl chloride in the form of label.

USE - For e.g. credit card used in contactless communication.

ADVANTAGE - The module is manufactured using metal lead frame which is cheaper than epoxy lead frame. The side and central sections of data carrier is made of conductive metal or its alloy, preferably a copper alloy which are comparatively flexible, thus, enables withstanding large load without causing adverse effects. The contact configuration requires only small height as central side sections of module are of less thickness.

DESCRIPTION OF DRAWING(S) - The figure is the sectional view of data carrier.

Recess (3)
Module (4)
Contact configuration (5)
Chip (6)
Chip cover (7)
Coplanar sides (16,17)
Central section (18)
Chip contacts (50,51)
Coil contacts (52,53)
Transmission coil (54)
Insulating layer (60)
pp; 16 DwgNo 2/2

8/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011592984

WPI Acc No: 1998-010112/199802

XRPX Acc No: N98-007876

Manufacture of smart cards - uses conducting tape to make contact between integrated circuit and external devices

Patent Assignee: GIESECKE & DEVRIENT GMBH (GIES-N)

Inventor: HOPPE J

Number of Countries: 004 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19621044	A1	19971127	DE 1021044	A	19960524	199802 B
EP 810547	A1	19971203	EP 97108394	A	19970523	199802

Priority Applications (No Type Date): DE 1021044 A 19960524

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
DE 19621044	A1	10	B42D-015/10	
EP 810547	A1 G	15	G06K-019/077	

Designated States (Regional): DE ES FR GB

Abstract (Basic): DE 19621044 A

The smart card (1) has a recess in which an **integrated circuit** (4) is located. A conducting tape (13) is applied to the card by means of a die (11) to make contact between the **integrated circuit** and the contact pads (2) or a coil (5) for **contactless communications**. The contacts on the **integrated circuit** have solder beads which are heated to make electrical contact with the tape. The tape consists of a transfer layer (13), a substrate (8), an insulating layer (7) and metallic contact pads (2). Alternatively, the pads can be coated with conducting adhesive (6) to stick to the **integrated circuit** contacts.

ADVANTAGE - Easily adaptable for different **integrated circuit** layouts.

Dwg.11/12

8/3,AB/4 (Item 3 from file: 350)
 DIALOG(R)File 350:Derwent WPIX
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009916043

WPI Acc No: 1994-183753/199422

XRPX Acc No: N94-145048

Stand-alone drive e.g. **IC chip credit card** for **wireless** powering and **communication** system - has inductor magnetically coupled to EM coupling medium and powered from energy pulses coupled to it by host system

Patent Assignee: XICOR INC (XICO-N)

Inventor: JAFFEE J M; OWEN W H; JAFFE J M

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9411842	A1	19940526	WO 93US9710	A	19931012	199422 B
US 5434396	A	19950718	US 92974131	A	19921110	199534
US 5502295	A	19960326	US 92974131	A	19921110	199618
			US 95420347	A	19950411	
EP 746824	A1	19961211	EP 93923837	A	19931012	199703
			WO 93US9710	A	19931012	
US 5587573	A	19961224	US 92974131	A	19921110	199706
			US 95432628	A	19950502	

Priority Applications (No Type Date): US 92974131 A 19921110; US 95420347 A 19950411; US 95432628 A 19950502

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
WO 9411842	A1 E	106	G06K-005/00	
US 5434396	A	51	G06K-005/00	
US 5502295	A	47	G06K-005/00	Div ex application US 92974131
				Div ex patent US 5434396
EP 746824	A1 E	106	G06K-005/00	Based on patent WO 9411842

Designated States (Regional): DE FR GB NL
US 5587573 A 47 G06K-005/00 Cont of application US 92974131
Cont of patent US 5434396

Abstract (Basic): WO 9411842 A

The stand-alone device (200) has an electromagnetic coupling medium (110). The electromagnetic coupling medium is capable of communicating data bi-directionally in the form of electromagnetic energy transitions. The energy transitions are coupled through the medium in the form of energy pulses.

The stand-alone device is formed on the substrate of an **integrated circuit chip** and includes an inductor. The stand-alone device is powered from the energy pulses coupled to it by the host system.

ADVANTAGE - Can be constructed in single **integrated circuit chip**, decreasing construction cost.

Dwg.3/16B

Abstract (Equivalent): US 5587573 A

A slave station formed on the substrate of an **integrated-circuit chip** for communicating with a master station which is coupled to said slave station by an electromagnetic coupling medium, the electromagnetic coupling medium being capable of communicating data bi-directionally between the master station and said slave station in the form of electromagnetic energy transitions, said energy transitions being coupled through said medium in the form of energy pulses, said slave station comprising:

an inductor means magnetically coupled to the coupling medium and including a segment of conductive material disposed on said substrate, a first terminal and a second terminal coupled at respective ends of said segment of conductive material, said inductor means for receiving magnetic energy transitions from the medium and for providing at said terminals an electrical signal indicative of said transitions;

means coupled to said inductor means for powering said slave station from the energy pulses coupled to said inductor means by said master station through said electromagnetic coupling medium; and

a communication means for selectively emitting at least one energy transition into said electromagnetic coupling medium in a selected time interval.

Dwg.1/16

US 5502295 A

A system for data transmission between a master station and a slave station in which an electromagnetic coupling medium is formed between the master station and the slave station, the electromagnetic coupling medium being capable of communicating data bi-directionally between the master station and the slave station in the form of electromagnetic energy transitions, said system comprising:

means in said master station for transmitting a first digital value to said slave station, including means for causing a first predetermined number of energy transitions to be coupled to said medium followed by a first resting duration in which substantially no energy transitions are coupled to said medium by said master station, said energy transitions being coupled through said medium in the form of energy pulses, each said energy pulse having a first energy level, a second energy level, and energy transitions between said first and second energy levels;

means in said master station for transmitting a second digital value to said slave station, including means for causing a second predetermined number of energy transitions to be coupled to said medium followed by a second resting duration in which substantially no energy transitions are coupled to said medium by said master station;

means in said slave station for detecting from said medium said first predetermined number of energy transitions followed by said first resting duration and for outputting a signal representative of said first digital value in response thereto, and for detecting said second predetermined number of energy transitions followed by said second resting duration and for outputting a signal representative of said second digital value in response thereto; and

means in said slave station for powering said slave station from the energy pulses coupled to it by said master station through said electromagnetic coupling medium.

Dwg.1/16b

US 5434396 A

The communication system has the capabilities of bi-directional data communications between the host and the stand-alone device and of powering the stand-alone device with energy pulses coupled through the electromagnetic coupling medium from the host. The electromagnetic medium is capable of supporting the bi-directional flow of energy pulses and energy transitions between the host and stand-alone device.

In one embodiment, bi-directional communication is provided by transmitting and detecting predetermined numbers of consecutive energy transitions coupled through the medium. Resting durations immediately precede and follow each predetermined number of consecutive energy transitions.

ADVANTAGE - Improved reliability.

10/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010544146

WPI Acc No: 1996-041099/199605

XRPX Acc No: N96-034494

Multilayer **chip card** coil for contactless **chip**

cards - has individual coils carried as conducting track windings
on mechanically flexible carrier elements combined to form folded flat
strip

Patent Assignee: ANGEWANDTE DIGITAL ELEKTRONIK (ANGE-N)

Inventor: KREFT H

Number of Countries: 061 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4428732	C1	19960104	DE 4428732	A	19940815	199605 B
WO 9605572	A1	19960222	WO 95DE1052	A	19950804	199614
AU 9532191	A	19960307	AU 9532191	A	19950804	199624
DE 19580862	T	19990415	DE 1080862	A	19950804	199921
			WO 95DE1052	A	19950804	

Priority Applications (No Type Date): DE 4428732 A 19940815

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

DE 4428732 C1 4 G06K-019/077

WO 9605572 A1 G 9 G06K-019/077

Designated States (National): AM AT AU BB BG BR BY CA CH CN CZ DE DK EE
ES FI GB GE HU JP KE KG KP KR KZ LK LR LT LU LV MD MG MN MW MX NO NZ PL
PT RO RU SD SE SI SK TJ TT UA US UZ VN

Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT KE LU MC
MW NL OA PT SD SE SZ UG

AU 9532191 A G06K-019/077 Based on patent WO 9605572

DE 19580862 T G06K-019/077 Based on patent WO 9605572

Abstract (Basic): DE 4428732 C

The coil is embedded in the plastic of the **chip card**.

Individual coils (9,10) are carried in the form of conducting track
windings on mechanically flexible carrier elements combined to form a
flat strip.

When the strip is folded together at marked positions (17) the
inductance of the coils laid one on top of the other is increased,
whereby holes formed in the foil at defined, repetitive positions, can
be used to make electrical connections to the coils.

USE/ADVANTAGE - For transferring electromagnetic signals and power
between **chip cards** and **external equipment**. Coil
arrangements can be simply made and their effect combined by electrical
connection. Optimal use is made of limited space in **chip**
card.

Dwg.1/4

12/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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05331708
NONCONTACT IC CARD AND ITS MANUFACTURE

PUB. NO.: 08-287208 [JP 8287208 A]
PUBLISHED: November 01, 1996 (19961101)
INVENTOR(s): ORIHARA KATSUHISA
FUJIMOTO MASAHIRO
MONKAWA HARUO
KURITA HIDEYUKI
APPLICANT(s): SONY CHEM CORP [488106] (A Japanese Company or Corporation),
JP (Japan)
APPL. NO.: 07-113641 [JP 95113641]
FILED: April 13, 1995 (19950413)

ABSTRACT

PURPOSE: To connect the antenna coil of the noncontact IC card, which transmits information by using an induced electromagnetic field as a transmission medium, and an IC chip together without using any line when the antenna coil is formed by etching.

CONSTITUTION: Of the noncontact IC card including at least the IC chip 6 arranged on an insulating substrate 1 and the antenna coil 2 which is formed by etching, a connection terminal 2a (2b) of the antenna coil 2 and a connection bump 6a (6b) of the IC chip 6 are connected together directly on a face-down basis or wire bonding through an anisotropic conductive adhesive layer 5 without using any jumper line.

12/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013727986
WPI Acc No: 2001-212216/200122
XRPX Acc No: N01-151516

Conductor layer to laminate into chip card with
recesses formed at connector locations and filled with screen print paste
Patent Assignee: ORGA KARTENSYSTEME GMBH (ORGA-N)

Inventor: FANNASCH L

Number of Countries: 095 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19940480	A1	20010308	DE 1040480	A	19990826	200122 B
WO 200117011	A2	20010308	WO 2000DE2889	A	20000824	200122
DE 19940480	C2	20010613	DE 1040480	A	19990826	200134
AU 200076426	A	20010326	AU 200076426	A	20000824	200137
EP 1145301	A2	20011017	EP 2000965786	A	20000824	200169
			WO 2000DE2889	A	20000824	

Priority Applications (No Type Date): DE 1040480 A 19990826

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

DE 19940480 A1 8 G06K-019/077

WO 200117011 A2 G H01L-021/48

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA

CH CN CR CU CZ DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE
KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO
RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW

DE 19940480 C2 G06K-019/077
AU 200076426 A H01L-021/48 Based on patent WO 200117011
EP 1145301 A2 G H01L-021/48 Based on patent WO 200117011
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SI

Abstract (Basic): DE 19940480 A1

Abstract (Basic):

NOVELTY - **Chip card** has **conductor track carrier layer** (1) with several **conductor tracks** (2) forming coil applied by screen printing. Connected to conductor tracks are contact surfaces (3) wider than the narrow conductor tracks. At locations of contact surfaces carrier layer has recesses (4a,b,c) which are completely filled with screen print paste. Recesses have different depths so contact surfaces have different thicknesses.

DETAILED DESCRIPTION - INDEPENDENT CLAIM is included for procedure to manufacture **chip card**.

USE - **Chip card** construction to prevent damage to conductor tracks when cutting recess in board to insert **chip module** and other electronic elements.

ADVANTAGE - Prevents damage to conductor tracks when cutting recesses in board and uncovering of contact surfaces as provides thicker contact surfaces.

DESCRIPTION OF DRAWING(S) - Cross section of carrier **layer** for **conductor tracks**.

Conductor track carrier layer (1)
Conductor track (2)
Contact surface (3)
Recesses (4a,4b,4c)
Protective layer (10)
pp; 8 DwgNo 1/4

12/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 THOMSON DERWENT. All rts. reserv.

012275370

WPI Acc No: 1999-081476/199907.

XRPX Acc No: N99-058564

IC module on **card** - has antenna connected to **chip**, made by patterning **conductor film** on one surface

Patent Assignee: ROHM CO LTD (ROHL)

Inventor: HIRAI M; HORIO T; MIYATA O; UEDA S

Number of Countries: 023 Number of Patents: 015

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9859318	A1	19981230	WO 98JP2833	A	19980623	199907 B
JP 11011057	A	19990119	JP 97166318	A	19970623	199913
JP 11011058	A	19990119	JP 97166319	A	19970623	199913
JP 11011059	A	19990119	JP 97166320	A	19970623	199913
JP 11034550	A	19990209	JP 97192204	A	19970717	199916
JP 11034558	A	19990209	JP 97198037	A	19970724	199916
JP 11099782	A	19990413	JP 97265548	A	19970930	199925
JP 11134461	A	19990521	JP 97297427	A	19971029	199931

EP 952542	A1	19991027	EP 98929675	A	19980623	199950
			WO 98JP2833	A	19980623	
CN 1234887	A	19991110	CN 98801035	A	19980623	200012
US 6160526	A	20001212	WO 98JP2833	A	19980623	200067
			US 99242748	A	19990222	
KR 2000068288	A	20001125	WO 98JP2833	A	19980623	200130
			KR 99701432	A	19990222	
KR 330652	B	20020329	WO 98JP2833	A	19980623	200266
			KR 99701432	A	19990222	
EP 952542	B1	20031029	EP 98929675	A	19980623	200379
			WO 98JP2833	A	19980623	
DE 69819299	E	20031204	DE 619299	A	19980623	200404
			EP 98929675	A	19980623	
			WO 98JP2833	A	19980623	

Priority Applications (No Type Date): JP 97297427 A 19971029; JP 97166318 A 19970623; JP 97166319 A 19970623; JP 97166320 A 19970623; JP 97192204 A 19970717; JP 97198037 A 19970724; JP 97265548 A 19970930

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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WO 9859318	A1	J	58	G06K-019/00	
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Designated States (National): CN KR US

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU

MC NL PT SE

JP 11011057	A	7	B42D-015/10	
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JP 11011058	A	8	B42D-015/10	
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JP 11011059	A	11	B42D-015/10	
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JP 11034550	A	9	B42D-015/10	
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JP 11034558	A	8	B42D-015/10	
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JP 11099782	A	6	B42D-015/10	
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JP 11134461	A	7	G06K-019/077	
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EP 952542	A1	E	G06K-019/00	Based on patent WO 9859318
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Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI

LU MC NL PT SE

CN 1234887	A	G06K-019/00	
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US 6160526	A	H01L-023/02	Based on patent WO 9859318
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KR 2000068288	A	G06K-019/00	Based on patent WO 9859318
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KR 330652	B	G06K-019/00	Previous Publ. patent KR 2000068288
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Based on patent WO 9859318

EP 952542	B1	E	G06K-019/077	Based on patent WO 9859318
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Designated States (Regional): DE FR

DE 69819299	E	G06K-019/077	Based on patent EP 952542
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Based on patent WO 9859318

Abstract (Basic): WO 9859318 A

The IC module (A) incorporated in an IC card (B) is provided with a board (1), an IC chip (2) mounted on the board, and an antenna coil (3) electrically connected to the IC chip.

The antenna coil is constituted by patterning a conductor film on one surface of the board.

ADVANTAGE - Simplifies manufacture. Reduces thickness of IC module.

Dwg.8/40

12/3,AB/4 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 THOMSON DERWENT. All rts. reserv.

011752471

WPI Acc No: 1998-169381/199815

Related WPI Acc No: 1997-471058; 1998-111583

XRPX Acc No: N98-134431

Electrical and mechanical connection method for **chip card** module - uses non-conductive hot-melt adhesive applied to foil **layer** overlaid with **conductive layer** at electrical connection points.

Patent Assignee: PAV CARD GMBH (PAVC-N)

Inventor: WILM R

Number of Countries: 065 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9808191	A1	19980226	WO 97EP4427	A	19970813	199815 B
AU 9743798	A	19980306	AU 9743798	A	19970813	199830
EP 920676	A1	19990609	EP 97941936	A	19970813	199927
			WO 97EP4427	A	19970813	
EP 920676	B1	20011121	EP 97941936	A	19970813	200176
			WO 97EP4427	A	19970813	
DE 59706058	G	20020221	DE 506058	A	19970813	200221
			EP 97941936	A	19970813	
			WO 97EP4427	A	19970813	
ES 2167791	T3	20020516	EP 97941936	A	19970813	200239

Priority Applications (No Type Date): DE 1037214 A 19960912; DE 1033936 A 19960822; DE 1033938 A 19960822; DE 1033939 A 19960822; DE 1037213 A 19960912

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 9808191 A1 G 39 G06K-019/077

Designated States (National): AL AU BB BG BR CA CN CZ EE GE HU IL IS JP KP KR LK LR LT LV MG MK MN MX NO NZ PL RO SG SI SK TR TT UA US UZ VN

Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9743798 A G06K-019/077 Based on patent WO 9808191

EP 920676 A1 G G06K-019/077 Based on patent WO 9808191

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

EP 920676 B1 G G06K-019/077 Based on patent WO 9808191

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

DE 59706058 G G06K-019/077 Based on patent EP 920676

Based on patent WO 9808191

ES 2167791 T3 G06K-019/077 Based on patent EP 920676

Abstract (Basic): WO 9808191 A

The connection method is used for providing mechanical and electrical connections between a **chip card** module and a **card carrier** when the **chip card** module is placed in a locating recess in the latter, using a non-conductive hot-melt adhesive. The adhesive is applied to a foil layer and overlaid at the electrical contact points by a **conductive layer**, for forming the electrical connections between the **chip card** module and the **card carrier**. The mechanical and electrical connections are formed in a single step by applied pressure and heat.

USE - For smart **card** manufacture.

ADVANTAGE - One-step process for simultaneously providing mechanical and electrical connections.

Dwg.4/7

12/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 THOMSON DERWENT. All rts. reserv.

010960528

WPI Acc No: 1996-457477/199646.

XRPX Acc No: N96-385513

Non contact **IC card** transferring data via induction
electromagnetic field - has substrate with **IC chip** and
antenna coil formed by etching, coil connection terminal and **IC**
chip connection bump are interconnected face down via anisotropic
conductive adhesive layer, **chip** is positioned across
coil

Patent Assignee: SONY CHEM CORP (SONY)

Inventor: FUJIMOTO M; KURITA H; MONKAWA H; ORIHARA K

Number of Countries: 005 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 737935	A2	19961016	EP 96105737	A	19960411	199646 B
JP 8287208	A	19961101	JP 95113641	A	19950413	199703
US 5705852	A	19980106	US 96629565	A	19960409	199808

Priority Applications (No Type Date): JP 95113641 A 19950413

Patent Details:

Patent No	Kind	Lan. Pg	Main IPC	Filing Notes
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EP 737935	A2	E	13	G06K-019/077
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Designated States (Regional): DE FR GB

JP 8287208	A	7	G06K-019/07
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US 5705852	A	12	H01L-023/02
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Abstract (Basic): EP 737935 A

The non contact **IC card** comprises a substrate (S) with
an **IC chip** (6) and an antenna coil (2) formed by etching. A
coil connecting terminal and a connecting bump of the **IC**
chip are interconnected in a face down relationship via an
anisotropic **conductive adhesive layer**. The **IC**
chip is positioned across the coil.

ADVANTAGE - Connects etched antenna coil and **chip** without
jumper wires eliminating bending stress in jumper wires so less
production cost, highly reliable connection using anisotropic
conductive adhesive.

Dwg.1A/8

Abstract (Equivalent): US 5705852 A

The non contact **IC card** comprises a substrate (S) with
an **IC chip** (6) and an antenna coil (2) formed by etching. A
coil connecting terminal and a connecting bump of the **IC**
chip are interconnected in a face down relationship via an
anisotropic **conductive adhesive layer**. The **IC**
chip is positioned across the coil.

ADVANTAGE - Connects etched antenna coil and **chip** without
jumper wires eliminating bending stress in jumper wires so less
production cost, highly reliable connection using anisotropic
conductive adhesive.

Dwg.1b/8

12/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 THOMSON DERWENT. All rts. reserv.

010278782

WPI Acc No: 1995-180038/199524

XRAM Acc No: C95-083432

XRPX Acc No: N95-141315

Contactless **chip card**, linked to scanner - has a structured laminated assembly which avoids tension peaks especially on bending
Patent Assignee: MICHALK M (MICH-I); ~~ODS~~ OLDENBOURG DATENSYSYSTEME GMBH R (ODSO-N)

Inventor: MICHALK M

Number of Countries: 001 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4337921	A1	19950511	DE 4337921	A	19931106	199524 B
DE 4345419	A1	19970814	DE 4337921	A	19931106	199738
			DE 4345419	A	19931106	
DE 4345455	A1	19980226	DE 4337921	A	19931106	199814
			DE 4345455	A	19931106	
DE 4345473	A1	19980813	DE 4345455	A	19931106	199838 N
			DE 4345473	A	19931106	
DE 4337921	C2	19980903	DE 4337921	A	19931106	199839

Priority Applications (No Type Date): DE 4337921 A 19931106; DE 4345419 A 19931106; DE 4345455 A 19931106; DE 4345473 A 19931106

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4337921	A1		11	G06K-019/077	
DE 4345419	A1			G06K-019/077	Div ex application DE 4337921 Div ex patent DE 4337921
DE 4345455	A1			G06K-019/077	Div ex application DE 4337921 Div ex patent DE 4337921
DE 4345473	A1			G06K-019/077	Div ex application DE 4345455 Div ex patent DE 4345455
DE 4337921	C2			G06K-019/077	Div in patent DE 4345455

Abstract (Basic): DE 4337921 A

The contactless **chip card** has an antenna coil (7) and leads and/or contact points (10) on a **conductor path film** (6) of flexible and electrically insulating material. Each semiconductor **chip** is in a **chip** housing (1) centrally in the laminated structure of the **chip card**. A housing film (4) is in a central layer, of flexible and electrically insulating material, extending from the housing (1), for external electrical conductors (3) with the outer connections (5). Also claimed is a mfg. process where the connection points (5) are brought to a **chip** housing (1) for the external electrical conductors (3), with the contact points (10) of the **conductor film** (6). They are bonded by lamination.

USE - The **chip card** is linked to a scanner for data and energy transfer by induction, microwaves or a capacititive coupling.

ADVANTAGE - The **card** assembly is wholly symmetrical within the **chip card**, to avoid any peaks of tension especially when bending.

Dwg. 6/6

15/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 THOMSON DERWENT. All rts. reserv.

014142088

WPI Acc No: 2001-626299/200172

XRPX Acc No: N01-466885

Producing tag or **chip card** involves producing antenna or coil
by stamping out of electrically conducting flat foil, combining with
other layers including **chip** module

Patent Assignee: INTERLOCK AG (INTE-N); VOGT W (VOGT-I)

Inventor: VOGT W

Number of Countries: 032 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200173800	A1	20011004	WO 2001IB532	A	20010331	200172 B
DE 10016037	A1	20011018	DE 1016037	A	20000331	200172
EP 1269496	A1	20030102	EP 2001915614	A	20010331	200310
			WO 2001IB532	A	20010331	
US 20030112202	A1	20030619	WO 2001IB532	A	20010331	200341
			US 2002240509	A	20020930	
KR 2003022783	A	20030317	KR 2002713018	A	20020930	200350
CN 1432182	A	20030723	CN 2001810577	A	20010331	200365

Priority Applications (No Type Date): DE 1016037 A 20000331

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 200173800 A1 G .25 H01F-041/04
Designated States (National): BR CN IN JP KR US
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU
MC NL PT SE TR
DE 10016037 A1 B31D-001/02
EP 1269496 A1 G H01F-041/04 Based on patent WO 200173800
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI TR
US 20030112202 A1 H01Q-001/40
KR 2003022783 A G06K-019/077
CN 1432182 A H01F-041/04

Abstract (Basic): WO 200173800 A1

Abstract (Basic):

NOVELTY - The method involves producing an antenna or coil shape by
stamping it out of an electrically conducting flat foil and finally
combining it with other layers including an electronic **chip**
module. The **copper** or **aluminum** foil (11) is mounted on a
plastic bearer foil (12) and the resulting double foil is subjected to
the stamping process.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the
following: an arrangement for producing a tag, **chip card**,
ID **card**, transponder unit or similar containing an antenna or
coil.

USE - For producing a tag, **chip card**, ID **card**,
transponder unit or similar containing an antenna or coil for wireless
transfer of information to a remote receiver.

ADVANTAGE - The manufacture and mounting of the coil on the
chip card are drastically simplified and the costs are
significantly reduced.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic
representation of a **copper** or **aluminum** foil on a bearer
foil before and after successful stamping

copper or aluminum foil (11)
plastic bearer foil (12)
tool (13)
pp; 25 DwgNo 2/4

15/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011791305

WPI Acc No: 1998-208215/199819

XRPX Acc No: N98-165415

Contact-less **chip card** - comprises **chip card**
module mounted on lead frame and induction coil formed on carrier foil,
which is electrically connected to lead frame and **chip card**
module over coil pads and respective lead frame contacts

Patent Assignee: SIEMENS AG (SIEI)

Inventor: FISCHBACH R; FRIES M; HOUDEAU D; KIRSCHBAUER J

Number of Countries: 025 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19640260	A1	19980402	DE 1040260	A	19960930	199819 B
WO 9814904	A1	19980409	WO 97DE2120	A	19970918	199821

Priority Applications (No Type Date): DE 1040260 A 19960930

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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DE 19640260	A1	5	G06K-019/077		
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WO 9814904	A1	G	12	G06K-019/077	
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Designated States (National): BR CN JP KR MX RU UA US

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC
NL PT SE

Abstract (Basic): DE 19640260 A

The **chip card** comprises a **chip card** module
mounted on a lead frame (1) and contacted to it, and an induction coil
(3) formed on a carrier foil (8) for a data transmission. The coil is
electrically connected to the lead frame and the **chip card**
module over coil pads (7) and respective lead frame contacts (4).

The connection between the lead frame contacts and the coil pads
arranged on an opposite side of the carrier foil, is formed by welding
or soldering of the coil pads to the lead frame contacts projecting
through break-through (5) in the carrier foil and the coil pads. The
coil pads are pref. arranged opposite a **chip** module window, and
the coil is formed of a structured **copper** layer.

ADVANTAGE - Provides improved and simplified positioning of pads
and construction.

Dwg.1/5

15/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010643538

WPI Acc No: 1996-140492/199615

XRAM Acc No: C96-044208

XRPX Acc No: N96-117659

Chip card module with antenna coil - with bond contacts for

antenna on carrier

Patent Assignee: SIEMENS AG (SIEI)

Inventor: HOUDEAU D; MUNDIGL J

Number of Countries: 024 Number of Patents: 014

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4431605	A1	19960307	DE 4431605	A	19940905	199615 B
WO 9607984	A1	19960314	WO 95DE1201	A	19950905	199617
FI 9700924	A	19970304	WO 95DE1201	A	19950905	199723
			FI 97924	A	19970304	
EP 780006	A1	19970625	EP 95929753	A	19950905	199730
			WO 95DE1201	A	19950905	
DE 4431605	C2	19980604	DE 4431605	A	19940905	199826
JP 10505023	W	19980519	WO 95DE1201	A	19950905	199830
			JP 96509119	A	19950905	
KR 97705803	A	19971009	WO 95DE1201	A	19950905	199841
			KR 97701445	A	19970305	
US 5809633	A	19980922	US 97812111	A	19970305	199845
EP 780006	B1	19981118	EP 95929753	A	19950905	199850
			WO 95DE1201	A	19950905	
DE 59504285	G	19981224	DE 504285	A	19950905	199906
			EP 95929753	A	19950905	
			WO 95DE1201	A	19950905	
ES 2125650	T3	19990301	EP 95929753	A	19950905	199916
RU 2155379	C2	20000827	WO 95DE1201	A	19950905	200103
			RU 97105182	A	19950905	
CN 1160447	A	19970924	CN 95195671	A	19950905	200143
KR 358785	B	20030421	WO 95DE1201	A	19950905	200355
			KR 97701445	A	19970305	

Priority Applications (No Type Date): DE 4431605 A 19940905

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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DE 4431605	A1		3	H01L-021/60	
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WO 9607984	A1 G		9	G06K-019/077	
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Designated States (National): CN FI JP KR RU UA US

Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL

PT SE

FI 9700924	A			G06K-000/00	
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EP 780006	A1 G			G06K-019/077	Based on patent WO 9607984
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Designated States (Regional): AT CH DE ES FR GB GR IT LI SE

DE 4431605	C2			H01L-021/60	
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JP 10505023	W		7	B42D-015/10	Based on patent WO 9607984
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KR 97705803	A			G06K-019/077	Based on patent WO 9607984
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US 5809633	A			H02P-011/00	
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EP 780006	B1 G			G06K-019/077	Based on patent WO 9607984
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Designated States (Regional): AT CH DE ES FR GB GR IT LI SE

DE 59504285	G			G06K-019/077	Based on patent EP 780006
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Based on patent WO 9607984

ES 2125650	T3			G06K-019/077	Based on patent EP 780006
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RU 2155379	C2			G06K-019/077	Based on patent WO 9607984
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CN 1160447	A			G06K-019/077	
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KR 358785	B			G06K-019/077	Previous Publ. patent KR 97705803
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Based on patent WO 9607984

Abstract (Basic): DE 4431605 A

A flat carrier (1) of flexible, non-conducting material has a recess (2) into which a semiconductor chip (3) is inserted. The chip has two contact areas (4) with connections (6) for an antenna coil (5), mfd. from lacquer-insulated Al wire. Wire is

bonded to one contact area, then coiled by a coil winder integrated in the bonder before being bonded to the other contact. The **chip** is put in the recess and the antenna is located on the carrier.

ADVANTAGE - **Chip card** module for a contactless **chip card** is made simply by automatable process.

Dwg.1/1

? DS

17/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011626392

WPI Acc No: 1998-043520/199805

XRAM Acc No: C98-014794

XRPX Acc No: N98-034712

Non-contact smart **card** used in private and public life - carries
antenna tracks adhesively held and formed into precisely aligned contact
bumps in single stage hot stamping, to which microcircuit **chips** are
flip-connected for hermetic encapsulation

Patent Assignee: FRAUNHOFER GES FOERDERUNG ANGEWANDTEN (FRAU); SMART PAC
GMBH TECHNOLOGY SERVICES (SMAR-N); ZAKEL E (ZAKE-I)

Inventor: ANSORGE F; ASCHENBRENNER R; KASULKE P; ZAKEL E

Number of Countries: 006 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19639902	A1	19971218	DE 1039902	A	19960927	199805 B
FR 2751452	A1	19980123	FR 977495	A	19970617	199811
WO 9923606	A1	19990514	WO 97EP6088	A	19971104	199926 N
DE 19639902	C2	20010301	DE 1039902	A	19960927	200112
JP 2001522107	W	20011113	WO 97EP6088	A	19971104	200207 N
			JP 2000519394	A	19971104	
US 6651891	B1	20031125	WO 97EP6088	A	19971104	200403 N
			US 2000530339	A	20000628	

Priority Applications (No Type Date): DE 1024119 A 19960617; WO 97EP6088 A
19971104; JP 2000519394 A 19971104; US 2000530339 A 20000628

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19639902	A1		7	G06K-019/077	
FR 2751452	A1		21	G06K-019/077	
WO 9923606	A1	G		G06K-019/077	
Designated States (National): JP KR SG US					
DE 19639902	C2			G06K-019/077	Div in patent DE 19732353
JP 2001522107	W		26	G06K-019/077	Based on patent WO 9923606
US 6651891	B1			G06K-019/00	Based on patent WO 9923606

Abstract (Basic): DE 19639902 A

The production of a novel, non-contact smart **card** (1) is
claimed. The **electrically-insulating**, flat **card** is
made with at least one recess(es) on one side. Conductive track(s) are
applied in a given pattern, on the surface of the recessed side. The
track(s) are applied on surfaces both within and outside the
recess(es). Microcircuit **chip**(s) (4) are aligned in the
recess(es) and brought into contact with the track(s).

Also claimed is a contact-less smart **card**, essentially as
described.

USE - Used to make a contact-less smart **card** with potentially
extremely wide application in private and public life.

ADVANTAGE - The process manufactures non-contact smart **cards**,
producing the coils especially, at low cost. Resistance to mechanical
stress and reliability are good. Single stage processes are employed
where possible. Hot Stamp coil application is particularly economic and
adhesive on the coil underside completes attachment.

High production rates are achieved. The coil transfers data and/or
energy, acting as an antenna. Of various applicable mounting
technologies, the flip-**chip** method is particularly compact.
Contact bumps are conveniently and accurately formed and registered

during the earlier hot-stamping stage. Hermetic sealing using glob top technology, increases the reliable life of the card.

Dwg.4/4

17/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011408734

WPI Acc No: 1997-386641/199736

XRPX Acc No: N97-321777

Chip card for transmission of electrical signals to terminal
- includes semiconductor chip with coupling elements and conductor tracks carrier made of flexible material, e.g. polyimide

Patent Assignee: SIEMENS AG (SIEI)

Inventor: FRIES M; JANCZEK T

Number of Countries: 026 Number of Patents: 011

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19609636	C1	19970814	DE 1009636	A	19960312	199736	B
WO 9734255	A1	19970918	WO 97DE409	A	19970304	199743	
EP 886834	A1	19981230	EP 97915335	A	19970304	199905	
			WO 97DE409	A	19970304		
CN 1213450	A	19990407	CN 97193006	A	19970304	199932	
JP 11508074	W	19990713	JP 97532179	A	19970304	199938	
			WO 97DE409	A	19970304		
BR 9710162	A	19990928	BR 9710162	A	19970304	200005	
			WO 97DE409	A	19970304		
US 6020627	A	20000201	WO 97DE409	A	19970304	200013	
			US 98152829	A	19980914		
MX 9807401	A1	19990201	MX 987401	A	19980911	200055	
KR 99087643	A	19991227	WO 97DE409	A	19970304	200059	
			KR 98707096	A	19980909		
RU 2170457	C2	20010710	WO 97DE409	A	19970304	200147	
			RU 98118496	A	19970304		
MX 208117	B	20020603	WO 97DE409	A	19970304	200366	
			MX 987401	A	19980911		

Priority Applications (No Type Date): DE 1009636 A 19960312

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

DE 19609636 C1 7 G06K-019/077

WO 9734255 A1 G 21 G06K-019/077

Designated States (National): BR CN JP KR MX RU UA US

Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC
NL PT SE

EP 886834 A1 G G06K-019/077 Based on patent WO 9734255

Designated States (Regional): AT CH DE ES FR GB IT LI

CN 1213450 A G06K-019/077

JP 11508074 W 14 G06K-019/077 Based on patent WO 9734255

BR 9710162 A G06K-019/077 Based on patent WO 9734255

US 6020627 A H01L-023/02 Cont of application WO 97DE409

MX 9807401 A1 G06K-019/077

KR 99087643 A G06K-019/077 Based on patent WO 9734255

RU 2170457 C2 G06K-019/077 Based on patent WO 9734255

MX 208117 B G06K-019/077

Abstract (Basic): DE 19609636 C

The chip card has a card body containing a

coupling element with conductor tracks and contacts and a semiconductor **chip**. The semiconductor **chip** includes an electronic circuit connected to a coupling element.

A carrier supporting at least one portion of the conductor tracks and the contacts of the coupling element is made of an **electrically insulating material**. The carrier has an opening in the region of the contacts and is made of temp. stable flexible material, e.g. polyimide. The electrically effective surface of the coupling element is at least close to the entire surface of the **chip card**.

USE/ADVANTAGE - **Chip card** manufacture, e.g. for telephone **cards**. Simple mounting of coupler elements with semiconductor **chip**. Highly reliable, long life.

Dwg.1/2

17/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008315524

WPI Acc No: 1990-202525/199027

XRPX Acc No: N90-157636

Integrated circuit module for electronic **card** or key -
has small dimension **integrated circuit** enclosed in annular
winding both engaged in insulating hardened adhesive
Patent Assignee: ETA SA (EBAU); ETA FAB EBAUCHES SA (EBAU)
Inventor: STAMPFLI J
Number of Countries: 010 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat.No	Kind	Date	Week
EP 376062	A	19900704	EP 89123010	A	19891213	199027 B
FR 2641102	A	19900629				199033
US 4999742	A	19910312	US 89455011	A	19891222	199113
EP 376062	B1	19950215	EP 89123010	A	19891213	199511
DE 68921179	E	19950323	DE 621179	A	19891213	199517
			EP 89123010	A	19891213	

Priority Applications (No Type Date): FR 8817210 A 19881227

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 376062	A			

Designated States (Regional): AT CH DE GB IT LI NL SE

EP 376062 B1 F 19 G06K-019/06

Designated States (Regional): AT CH DE GB IT LI NL SE

DE 68921179 E G06K-019/06 Based on patent EP 376062

Abstract (Basic): EP 376062 A

The electronic module has a substrate of insulating material (24), an **integrated circuit** (8) fitted with at least two connection terminals (10), which is indirectly fixed to the substrate. A winding (12) is also fixed on the substrate to permit inductive coupling between the module and a device with which the portable object is fitted. Electrical connections (18,20) connect the winding to **integrated circuit**.

The winding has an annular form and it surrounds a space in which the whole of the **integrated circuit** and its connections are placed and which is filled with an **electrically insulating** and hardened adhesive.

ADVANTAGE - Can be mass-produced at low cost after which it is

inserted into winding which ensures protection. (16pp Dwg.No.7/14
Abstract (Equivalent): EP 376062 B

Electronic module for a small portable object such as a **card** or a key having an **integrated circuit**, comprising a substrate of **electrically insulating material** (24; 54) a substantially parallelepipedic **integrated circuit chip** (8; 36) having a front surface provided with at least two connector lugs (10; 38) and a back surface and which is at least indirectly fixed to said substrate, a coil (12; 40) having two terminals (17; 43) and also fixed on said substrate for enabling inductive coupling of the module (22; 60) and an apparatus with which said object can cooperate, and respective electrical connections (18, 20; 46) between the **chips**'s connector lugs and the coil's terminals, said coil having an annular form and surrounding a space in which said **chip** and said electrical connections are housed, characterized by the fact that said coil has a height higher than the thickness of said **chip** and by the fact that said space is filled with an hardened, **electrically insulating adhesive material** (28; 58) so that the coil forms a protective structure of said **chip**.

Dwg.1/14

Abstract (Equivalent): US 4999742 A

The electronic module includes a substrate (24) of insulating material.

An **integrated circuit chip** (8) having at least two connector lugs (10) is fixed at least indirectly to the substrate.

A coil (12) is also fixed on the substrate and serves to provide an inductive coupling between the module and an appts. with which the portable object is designed to cooperate. Electrical connections (18,20) are provided respectively between the **chip**'s connector lugs and the terminals (17) of the coil. The coil is an annular coil which surrounds a space in which the **chip** and the electrical connections are fully housed in a hardened, **electrically insulating adhesive material** (28) filling the space.

USE/ADVANTAGE - For small portable object such as **card** or key incorporating **integrated circuit**.

May be mass produced at low cost and, when it is then incorporated in **card**, coil effectively protects **chip** and electrical connections against any constraints to which **card** is submitted.

(12pp

17/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004770036

WPI Acc No: 1986-273377/198642

XRAM Acc No: C86-118269

XRPX Acc No: N86-204076

Electronic modules mfr. for microcircuit **cards** - by preparing connector grid and IC **chip** and soldering **chip** leads to tongues on grid

Patent Assignee: ETA FAB EBAUCHES SA (EBAU)

Inventor: STAMPFLI J M; STAMPFLI J

Number of Countries: 011 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 197438	A	19861015	EP 86104178	A	19860326	198642 B
FR 2579798	A	19861003	FR 855109	A	19850402	198646

JP 61232629	A	19861016	JP 8674404	A	19860402	198648
US 4674175	A	19870623	US 86846936	A	19860401	198727
EP 197438	B	19900620				199025
DE 3672171	G	19900726				199031
EP 197438	B2	19950823	EP 86104178	A	19860326	199538

Priority Applications (No Type Date): FR 855109 A 19850402

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

EP 197438 A F 19

Designated States (Regional): AT CH DE GB IT LI NL SE

EP 197438 B

Designated States (Regional): AT CH DE GB IT LI NL SE

EP 197438 B2 F 22 G06K-019/06

Designated States (Regional): AT CH DE GB IT LI NL SE

Abstract (Basic): EP 197438 B

Use of electronic modules for microcircuit **cards** each comprising an **IC chip** with a front face provided with connecting leads and a rear face, and an assembly of metallic contact areas each connected to one of the connecting leads of **chip**, is claimed.

(a) A metal grid (1) is provided including a number of identical openings (2) delimited by a frame (4) and in each opening an assembly of tongues (3) attached to the frame for forming the contact area of a module; (b) a series of pellets (6) is provided made from plastics material smaller than the openings in the grid, each pellet having a flat front surface (6a), a rear surface on the side of which is an opening (8) and between the opening and the front surface, windows (9) provided so as to be able to bring each one at right angles to a tongue in an assembly; (c) a pellet is fixed by its front face onto each assembly of tongues so that the windows are at right angles to the tongues; (d) an **IC chip** (12) is fixed to the bottom of the opening of each pellet so that its back surface is oriented towards the grid; (e) the connecting leads (13) of the **chip** are connected to tongues to which the pellet is fixed by means of conductors lodged in the opening of the pellet and passing through the windows; and (f) the opening and the windows of each pellet are filled with a hardenable adhesive (15) which is **electrically insulating**.

USE - The microcircuit **cards** are used as credit **cards**, banker's **cards**, parking **cards**, payment **cards** for public telephones, etc. (19pp Dwg.No.2C-3/15)

Abstract (Equivalent): EP 197438 B

A process for fabricating electronic modules for microcircuit **cards**, each module comprising an **integrated circuit chip** with a front face provided with connecting terminals and a rear face and a set of metal contact areas each connected to one of the **chip's** connecting terminals, said process being characterized in that it comprises the following steps: -providing a metal grid (1;1') comprising a plurality of identical openings (2;2') defined by a frame (4;4') and, in each opening, a set of tongues (3;3') attached to the frame for forming the contact areas of a module; providing a series of pellets (6;6') of synthetic material, these being smaller than the openings in the grid and each one having a generally flat front face (6a;6a'), a rear face (6b;6b') in which there is located a hollow (8;8') and, between this hollow and said front face, windows (9;9') so arranged that they can be positioned opposite the tongues respectively of one of said sets of tongues; -attaching a pellet by its front face to each set of tongues in such a way that said windows are actually opposite these tongues; -attaching an **integrated**

circuit chip (12;12') to the bottom of said hollow in each said attached pellet so that the rear face of said **integrated circuit** is directed towards the said grid;-connecting said **chip's** connecting terminals (13;13') to said tongues to which said pellet is attached by means of conductors (14;14') located in the hollow in said pellet and passing through said windows; and filling said hollow and said windows in each said pellet with an **electrically insulating**, hardenable, adhesive material (15;15'). (20pp)

Abstract (Equivalent): US 4674175 A

Electronic modules for microcircuit **cards** are mfd. by attaching synthetic pellets to one of a set of tongues attached to a frame formed by a metal grid; and attaching an **integrated circuit chip** to the bottom of a hollow in each pellet. The **chips'** terminals are attached by conductors extending through windows to the tongues. The hollow and the windows are filled with **electrically insulating** adhesive material.

ADVANTAGE - Prodn. costs of **cards** are reduced. (13pp)r

? DS

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2004/Feb W5

(c) 2004 Institution of Electrical Engineers

*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

File 6:NTIS 1964-2004/Mar W1

(c) 2004 NTIS, Intl Cpyrght All Rights Res

File 8:Ei Compendex(R) 1970-2004/Feb W5

(c) 2004 Elsevier Eng. Info. Inc.

File 34:SciSearch(R) Cited Ref Sci 1990-2004/Mar W1

(c) 2004 Inst for Sci Info

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

(c) 1998 Inst for Sci Info

File 35:Dissertation Abs Online 1861-2004/Feb

(c) 2004 ProQuest Info&Learning

File 65:Inside Conferences 1993-2004/Mar W1

(c) 2004 BLDSC all rts. reserv.

File 94:JICST-EPlus 1985-2004/Feb W5

(c)2004 Japan Science and Tech Corp(JST)

File 99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb

(c) 2004 The HW Wilson Co.

File 144:Pascal 1973-2004/Feb W5

(c) 2004 INIST/CNRS

File 305:Analytical Abstracts 1980-2004/Mar W1

(c) 2004 Royal Soc Chemistry

*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.

File 315:ChemEng & Biotec Abs 1970-2004/Feb

(c) 2004 DECHEMA

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200416

(c) 2004 THOMSON DERWENT

File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)

(c) 2004 JPO & JAPIO

*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.

File 344:Chinese Patents Abs Aug 1985-2004/Mar

(c) 2004 European Patent Office

File 371:French Patents 1961-2002/BOPI 200209

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*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	8019	AU=(KAWAMURA, S? OR KAWAMURA S?)
S2	17687	AU=(SHIMIZU, S? OR SHIMIZU S?)
S3	2	S1 AND S2
S4	2	RD (unique items)
S5	25704	S1:S2
S6	757	S5 AND ((INTEGRAT?(3N)(CIRCUIT? OR LOOP? ?)) OR IC OR CHIP? ?)
S7	59	S6 AND ((INTEGRAT?()CIRCUIT? OR IC)(3N)ELEMENT? ? OR CARD? ?)
S8	0	S7 AND ((COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE?- ???) (3N)COMPOSIT?)
S9	0	S7 AND (CONTACTLESS OR WIRELESS) (3N)COMMUNICAT??????
S10	7	S7 AND (ELECTROLESS(2N)(PLATING OR PLATE??? OR COVER? OR C- OAT?) OR ELECTROPLAT????? OR ELECTRO()(PLATING OR PLATE??? OR COVER? OR COAT?) OR ELECTROFORM??????? OR ELECTROFORM??????)
S11	4	RD (unique items)
S12	52	S7 NOT S10
S13	0	S12 AND (ALUMINUM OR AL OR NICKEL OR NI OR COPPER OR CU OR CHROMIUM OR CR)
S14	0	S12 AND (COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE?- ???) (3N)PATTERN?
?		

4/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014122861

WPI Acc No: 2001-607073/200169

XRPX Acc No: N01-453177

Information input/output unit containing two types of non-contact
information media and a radio antenna

Patent Assignee: HITACHI MAXELL KK (HITM)

Inventor: INOSE F; KANEKO T; **KAWAMURA S**; **SHIMIZU S**

Number of Countries: 094 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200137213	A1	20010525	WO 2000JP7901	A	20001109	200169 B
AU 200113043	A	20010530	AU 200113043	A	20001109	200169
JP 2001202483	A	20010727	JP 2000342325	A	20001109	200169
EP 1231562	A1	20020814	EP 2000974878	A	20001109	200261
			WO 2000JP7901	A	20001109	
CN 1390334	A	20030108	CN 2000815523	A	20001109	200334

Priority Applications (No Type Date): JP 99323456 A 19991112

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 200137213 A1 J 45 G06K-017/00

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA
CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS KE
KG KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU
SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200113043 A G06K-017/00 Based on patent WO 200137213

JP 2001202483 A 14 G06K-017/00

EP 1231562 A1 E G06K-017/00 Based on patent WO 200137213

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI

CN 1390334 A G06K-017/00

Abstract (Basic): WO 200137213 A1

Abstract (Basic):

NOVELTY - Notebook personal computer (300) has attached
reader/writer (100) that takes up two types of noncontact information
media of different shapes (202,204) and has an antenna to communicate
with noncontact information media by radio. Communication with a
contact-type noncontact information medium can be reliably effected,
preferably with a specified degree of freedom of the shape of the
medium.

USE - Information input/output unit containing two types of
non-contact information media and a radio antenna

DESCRIPTION OF DRAWING(S). - Diagram of computer with input/output
device.

Read/write unit (100)

IC card (202)

IC tag (204)

Notebook computer (300)

pp; 45 DwgNo 1/24

4/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

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013627770

WPI Acc No: 2001-111978/200112

XRPX Acc No: N01-082259

IC device, e.g. for contactless data carrier, has multilayer structure
with metallized layers forming coil around storage chip

Patent Assignee: HITACHI MAXELL KK (HITM)

Inventor: KAWAMURA S; SHIMIZU S

Number of Countries: 090 Number of Patents: 009

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200051181	A1	20000831	WO 2000JP1029	A	20000223	200112 B
AU 200026904	A	20000914	AU 200026904	A	20000223	200112
JP 2000323643	A	20001124	JP 200044765	A	20000222	200112
EP 1193759	A1	20020403	EP 2000905288	A	20000223	200230
			WO 2000JP1029	A	20000223	
KR 2002005596	A	20020117	KR 2001710800	A	20010823	200250
JP 3347138	B2	20021120	JP 200044765	A	20000222	200282
			JP 200210220	A	20000222	
JP 2002319012	A	20021031	JP 200044765	A	20000222	200304
			JP 200210230	A	20000222	
JP 2002324890	A	20021108	JP 200044765	A	20000222	200305
			JP 200210220	A	20000222	
JP 2002343877	A	20021129	JP 200044765	A	20000222	200309
			JP 200220219	A	20000222	

Priority Applications (No Type Date): JP 9959753 A 19990308; JP 9946545 A
19990224

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200051181	A1	J	41	H01L-025/00	Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS KE KG KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
AU 200026904	A			H01L-025/00	Based on patent WO 200051181
JP 2000323643	A		14	H01L-025/00	
EP 1193759	A1	E		H01L-025/00	Based on patent WO 200051181
					Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
KR 2002005596	A			H01L-025/00	
JP 3347138	B2		11	H01L-025/00	Div ex application JP 200044765 Previous Publ. patent JP 2002324890
JP 2002319012	A		11	G06K-019/077	Div ex application JP 200044765
JP 2002324890	A		14	H01L-025/00	Div ex application JP 200044765
JP 2002343877	A		11	H01L-021/822	Div ex application JP 200044765

Abstract (Basic): WO 200051181.A1

Abstract (Basic):

NOVELTY - The IC device includes a conductor constituting a coil
(3) and having a multilayer structure comprising a sputtered or vapor
deposited metal layer and a metal plating layer which may be formed by
precision electrocasting. The information carrier includes an IC device
(1) disposed at the planar center of a base. The carrier may be
produced by mounting a required part including an IC device on a
band-form base and punching the base to produce the required individual
units.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for:

- (1) an IC device production method;
- (2) an information carrier mounted with an IC device;
- (3) and a production method for an information carrier mounted with an IC device.

USE - As a contactless data carrier interrogated via e.g. an inductive link.

ADVANTAGE - The IC device has an improved communication range for reading and writing into the information carrier.

pp; 41 DwgNo 1A/22

11/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7623041 INSPEC Abstract Number: B2003-06-2575F-030
Title: **Electroplating** Ni micro-cantilevers for low contact-force
IC probing
Author(s): Kataoka, K.; Kawamura, S.; Itoh, T.; Ishikawa, K.;
Honma, H.; Suga, T.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Univ. of Tokyo,
Japan
Journal: Sensors and Actuators A (Physical) vol.A103, no.1-2 p.
116-21
Publisher: Elsevier,
Publication Date: 15 Jan. 2003 Country of Publication: Switzerland
CODEN: SAAPEB ISSN: 0924-4247
SICI: 0924-4247(20030115)A103:1/2L116:EMCC;1-D
Material Identity Number: N866-2003-002
U.S. Copyright Clearance Center Code: 0924-4247/03/\$30.00
Language: English
Abstract: We present a new MEMS probe card made of
electroplated nickel micro-cantilevers, which has compliant
structures, and uses a kind of electric breakdown, or fritting, to make
electric contacts to electrodes on ICs. The characteristics of fritting
contact between nickel probe and Al electrodes were investigated, and
nickel was found to have lower contact resistance than other materials. A
micro-machining process for the probe cards, including deposition of
layers having different internal stress to make a protruding cantilever
shape, was developed. It was found that the fritting process using the
micro-cantilevers could make the low-resistance contacts with the force of
less than a few micronewtons.
Subfile: B
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11/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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7327952 INSPEC Abstract Number: B2002-08-2575F-088
Title: Low contact-force and compliant MEMS probe card utilizing
fritting contact
Author(s): Kataoka, K.; Kawamura, S.; Itoh, T.; Suga, T.; Ishikawa,
K.; Honma, H.
Author Affiliation: Res. Center for Adv. Sci. & Technol., Univ. of Tokyo,
Japan
Conference Title: Technical Digest. MEMS 2002 IEEE International
Conference. Fifteenth IEEE International Conference on Micro Electro
Mechanical Systems (Cat. No.02CH37266) p.364-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA xliii+737 pp.
ISBN: 0 7803 7185 2 Material Identity Number: XX-2002-00446
U.S. Copyright Clearance Center Code: 0-7803-7185-2/02/\$10.00
Conference Title: Technical Digest. MEMS 2002 IEEE International
Conference. Fifteenth IEEE International Conference on Micro Electro
Mechanical Systems
Conference Sponsor: IEEE; Robotics & Autom. Soc
Conference Date: 20-24 Jan. 2002 Conference Location: Las Vegas, NV,
USA
Language: English

Abstract: We present a new MEMS probe card made of electroplated Ni micro-cantilevers, which has compliant structures, and uses a kind of electric breakdown, or fritting, to make electric contacts to electrodes on ICs. The characteristics of fritting contact between Ni probe and Al electrodes were investigated, and Ni was found to have lower contact resistance than other materials. A micro-machining process for the probe cards, including deposition of layers having different internal stress to make a protruding cantilever shape, was developed.

Subfile: B

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11/3,AB/3 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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05098578 JICST ACCESSION NUMBER: 02A0240021 FILE SEGMENT: JICST-E
Coil on Chip RFID System by Super EF2 Technology.

KAWAMURA SATOSHI (1)

(1) Hitachi Maxell, Ltd.

Nippon Oyo Jiki Gakkai Kenkyukai Shiryo, 2002, VOL.123rd, PAGE.21-25,
FIG.12, TBL.3, REF.1

JOURNAL NUMBER: Z0979AAS ISSN NO: 1340-7562

UNIVERSAL DECIMAL CLASSIFICATION: 621.318.1

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Conference Proceeding

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: Hitachi Maxell has developed a Super Electro Fine Forming technology (Super EF2), which enables us have a high precision processes at Mm level. By use of the Supper EF2 technology, Coil on Chip RFID chip has been developed by mounting the micro-coil directly on the surface of each IC chip in a wafer. We succeeded in developing a Coil on Chip RFID system that can be applied in various close-coupled RFID solutions, which features in small size, low price as well as high reliability.
(author abst.)

11/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07456375

IC ELEMENT AND ITS MANUFACTURING METHOD

PUB. NO.: 2002-324890 [JP 2002324890 A]

PUBLISHED: November 08, 2002 (20021108)

INVENTOR(s): SHIMIZU SHIN

KAWAMURA TETSUSHI

APPLICANT(s): HITACHI MAXELL LTD

APPL. NO.: 2002-010220 [JP 200210220]
Division of 2000-044765 [JP 200044765]

FILED: February 22, 2000 (20000222)

PRIORITY: 11-046545 [JP 9946545], JP (Japan), February 24, 1999
(19990224)

11-059753 [JP 9959753], JP (Japan), March 08, 1999 (19990308)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a structure of an IC element that is suitable for manufacture of a non-contact communication type information carrier having a long communication distance, and to provide its manufacturing method.

SOLUTION: In the IC element, a conductor constituting an electric coil 3 has a multilayer structure that comprises a metal sputter layer or a metal evaporation layer 6 and a metal plating layer 7. In the method for manufacturing the IC element, precision electroforming is used as a means of forming a metal plating layer 7. The information carrier can be manufactured by arranging the IC element 1a at a center in a horizontal plane of a substrate 21, more particularly, by manufacturing what a required mounting component including the IC element is mounted on any one of belt-shaped materials 41-45 and then by forming by punching the required information carrier 20a to 20h from this belt-shaped material.

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STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact *the EIC searcher or contact:*

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

➤ I am an examiner in Workgroup: Example: 2810

➤ Relevant prior art **found**, search results used as follows:

- ☐ 102 rejection
- ☐ 103 rejection
- ☐ Cited as being of interest.
- ☐ Helped examiner better understand the invention.
- ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
(journal articles, conference proceedings, new product announcements etc.)

➤ Relevant prior art **not found**:

- ☐ Results verified the lack of relevant prior art (helped determine patentability).
- ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18



03/11/2004

09/914,077

11mar04 15:37:36 User267149 Session D1285.1

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2004/Feb W5

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File 6:NTIS 1964-2004/Mar W1

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File 8:EI Compendex(R) 1970-2004/Feb W5

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File 34:SciSearch(R) Cited Ref Sci 1990-2004/Mar W1

(c) 2004 Inst for Sci Info

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

(c) 1998 Inst for Sci Info

File 35:Dissertation Abs Online 1861-2004/Feb

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File 65:Inside Conferences 1993-2004/Mar W1

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File 94:JICST-EPlus 1985-2004/Feb W5

(c)2004 Japan Science and Tech Corp(JST)

File 99:Wilson Appl. Sci & Tech Abs 1983-2004/Feb

(c) 2004 The HW Wilson Co.

File 144:Pascal 1973-2004/Feb W5

(c) 2004 INIST/CNRS

File 305:Analytical Abstracts 1980-2004/Mar W1

(c) 2004 Royal Soc Chemistry

*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.

File 315:ChemEng & Biotec Abs 1970-2004/Feb

(c) 2004 DECHEMA

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200416

(c) 2004 THOMSON DERWENT

File 347:JAPIO Nov 1976-2003/Nov(Updated 040308)

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*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.

File 344:Chinese Patents Abs Aug 1985-2004/Mar

(c) 2004 European Patent Office

File 371:French Patents 1961-2002/BOPI 200209

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*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	1385141	(INTEGRAT?(3N) (CIRCUIT? OR LOOP? ?)) OR IC OR CHIP? ?
S2	263087	(INTEGRAT?())CIRCUIT? OR IC) (3N)ELEMENT? ? OR CARD? ?
S3	1590021	S1:S2
S4	12525	(COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE????) (3N)- COMPOSIT?
S5	41262	(COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE????) (3N)- (DIAMETER? OR WIDE??? OR WIDTH)
S6	20584	(RECTANGULAR? OR SQUARE??? OR ANGLE??? OR PERPENDICULAR?) (- 3N) (COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE????)
S7	15535	(COIL? ? OR SPIRAL???? OR CONCENTRIC????? OR WIRE????) (3N)- PATTERN?
S8	87242	S4:S7
S9	3896	CORNER? ?(3N) (CHAMFER? OR CUT OR CUT()OFF)
S10	61952	(CONTACTLESS OR WIRELESS) (3N)COMMUNICAT??????
S11	207671	DATA(3N)COMMUNICAT?????
S12	9262	(EXTERNAL??????? OR OUTSIDE) (3N)EQUIPMENT
S13	216585	S11:S12
S14	3612906	CONDUCT???????
S15	311225	CONDUCT???????(3N) (LAYER??? OR FILM??? OR COAT??? OR MULTIL- AYER??? OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER()LAYER????? OR MULTIPLE()LAYER? ?)
S16	24075	CONDUCT???????(3N) (ADJACENT??????? OR CLOSE OR NEAR OR ADJOI- N???????)
S17	3612906	S14:S16
S18	88410	METAL()SPUTTER? OR METAL()EVAPORAT? OR METAL()PLATE?
S19	4876122	ALUMINUM OR AL OR NICKEL OR NI OR COPPER OR CU OR CHROMIUM OR CR
S20	4949632	S18:S19
S21	70395	RESIST???????(3N)METAL?
S22	109764	ELECTROLESS(2N) (PLATING OR PLATE??? OR COVER? OR COAT?) OR ELECTROPLAT????? OR ELECTRO() (PLATING OR PLATE??? OR COVER? OR COAT?) OR ELECTROFORM????? OR ELECTROFORM??????
S23	271049	S10:S12
S24	4333	S3 AND S8
S25	3	S24 AND S9
S26	3	RD (unique items)
S27	4330	S24 NOT S25
S28	100	S27 AND S23
S29	6	S28 AND S17
S30	6	RD (unique items)
S31	94	S28 NOT S30
S32	2	S31 AND S20
S33	2	RD (unique items)
S34	92	S31 NOT S32
S35	0	S34 AND S21
S36	0	S34 AND S22
S37	16	S34 AND S2
S38	14	RD (unique items)
S39	76	S34 NOT S37
S40	1	S39 AND S4
S41	75	S39 NOT S40
S42	66	S41 AND S5
S43	1	S42 AND S6
S44	65	S42 NOT S43
S45	0	S44 AND S7
S46	64	S44 AND S10

03/11/2004

09/914,077

S47	12	S46 AND S11
S48	6	RD (unique items)
S49	52	S46 NOT S47
S50	0	S49 AND S12
S51	0	S49 AND S14
S52	0	S49 AND S18
S53	35	RD S49 (unique items)
S54	6383	S3 AND S22
S55	68	S54 AND S8
S56	67	S55 NOT S42,S37,S33,S30,S25
S57	40	S56 AND S20
S58	1	S57 AND S21
S59	39	S57 NOT S58
S60	16	S59 AND S17
S61	12	RD (unique items)
S62	23	S59 NOT S60
S63	0	S62 AND S9
S64	15	RD S62 (unique items)

26/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011203664

WPI Acc No: 1997-181588/199717

XRAM Acc No: C97-058642

XRPX Acc No: N97-149407

Antenna for pass or identity card transponder comprises magnetic core of composite material, which is wound with coil, and has small loss, including eddy current loss, at high frequency

Patent Assignee: MITSUBISHI MATERIALS CORP (MITV); ENDO T (ENDO-I);

MIYAKI M (MIYA-I); TSUCHIDA T (TSUC-I); YAHATA S (YAHA-I)

Inventor: ENDO T; MIYAKE M; TSUCHIDA T; YAHATA S; MIYAKI M

Number of Countries: 007 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 762535	A1	19970312	EP 96113479	A	19960822	199717 B
JP 10022722	A	19980123	JP 96176544	A	19960705	199814
JP 10075113	A	19980317	JP 96221310	A	19960822	199821
EP 762535	B1	19981104	EP 96113479	A	19960822	199848
TW 337621	A	19980801	TW 96109524	A	19960806	199849
DE 69600910	E	19981210	DE 600910	A	19960822	199904
			EP 96113479	A	19960822	
KR 98012707	A	19980430	KR 9634104	A	19960817	199917
US 20030107523	A1	20030612	US 96701457	A	19960822	200340

Priority Applications (No Type Date): JP 96176544 A 19960705; JP 95213353 A 19950822; JP 96176543 A 19960705

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 762535	A1	E	17	H01Q-007/06	
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Designated States (Regional): DE FR GB

JP 10022722	A		5	H01Q-007/06	
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JP 10075113	A		7	H01Q-007/06	
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EP 762535	B1	E		H01Q-007/06	
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Designated States (Regional): DE FR GB

TW 337621	A			H01Q-001/36	
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DE 69600910	E			H01Q-007/06	Based on patent EP 762535
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KR 98012707	A			H01Q-007/00	
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US 20030107523	A1			H01Q-001/00	
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Abstract (Basic): EP 762535 A

An antenna (6, 7, 9) for a transponder comprises a magnetic core (4) of a composite material and a coil (5) wound on the magnetic core.

Also claimed is a plate transponder (8) comprising 2 plate antennae (6, 7) composed of a wound conductor on a magnetic core (4) and an air-core antenna (9) composed of a spirally wound conductor.

The composite material comprises layered rectangular metallic thin plates, pref. 3-16 plates of an amorphous magnetic material of thickness 20-50 micron, which are insulated by oxidising their surfaces. The corners may be cut or rounded. The ratio of shorter side:longer side = 0.4-1.0. The antenna has a thickness of 0.4 mm or less. The coil conductor has a dia. of 100-200 micron. It is wound on the core perpendicular to the longer side. The magnetic core may be provided as a plate and the composite material may comprise magnetically soft flakes, pref. selected from pure iron, silicon steel, a permalloy (Fe-Ni) and an iron/cobalt amorphous alloy; and a synthetic

resin. Pref. are flakes of amorphous Co-Fe-Ni-B-Si of max. thickness 30 (10) micron and dia. 50-2000 (100-1000) micron. The resin is selected from thermoset epoxy, phenol, ureal unsatd. polyester and 4 named other resins, or from thermoplastic polyethylene, polypropylene, etc.

USE - As an ID **card**, a commuter pass or a coupon ticket, which operates at a frequency of over 100 kHz with a plate [magnetic flakes in a binder] magnetic core or at 40-200 kHz with a core comprising layered thin plates (claimed). The transponder is suitable for the above uses when operated at a frequency of 40-200 kHz (claimed).

ADVANTAGE - The antenna is thin and flexible, allowing it to be carried in a pocket, it has a small loss, including eddy current loss, at a high frequency and it is not affected by the proximity of coins, aluminium foil in a cigarette packet or other ferrous or non-ferrous metal materials, e.g keys for cars or buildings.

4A, 4B, 5A, 5

B/7

26/3, AB/2 (Item 1 from file: 347)
DIALOG(R) File 347: JAPIO
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06445768

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-031338 [JP 2000031338-A]
PUBLISHED: January 28, 2000 (20000128)
INVENTOR(s): OGAWA TOSHIO
TAKAHASHI MASA AKI
AIDA MASAHIRO
KAMIMURA NORITAKA
TANBA AKIHIRO
APPLICANT(s): HITACHI LTD
APPL. NO.: 10-196968 [JP 98196968]
FILED: July 13, 1998 (19980713)

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a power semiconductor device having low heat resistance and high voltage resistance by **chamfering** at least one **corner** section of its lead frame.

SOLUTION: The corner sections of a Cu lead frame 13 which is formed in a prescribed pattern and has a thickness of 0.7 mm are rounded with a radius of curvature R and an uncured resin sheet having a thickness of 0.15 mm is interposed between the main surface 2 of the lead frame 13 and a base substrate 15 in the forming process of the lead frame 13 by press work. Then a resin insulating layer 18 is constituted of the resin sheet by integrally thermocompression bonding the sheet and an IGBT **chip** is mounted on the other main surface 1 of the frame 13 as a semiconductor element 11. After mounting the IGBT **chip**, the **chip** is soldered to the main surface 1 and a main circuit is configured by electrically connecting the element 11 to the frame 13 through Al **wires** having a **diameter** of 0.3 mm. Therefore, the thickness of the resin insulating layer can be reduced without deteriorating the reliability and, consequently, the heat resistance from the semiconductor element 11 to the base substrate 15 can be reduced.

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26/3,AB/3 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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02171431
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 62-088331 [JP 62088331**A]
PUBLISHED: April 22, 1987 (19870422)
INVENTOR(s): KOYABU KUNIHIRO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 60-230203 [JP 85230203]
FILED: October 15, 1985 (19851015)
JOURNAL: Section: E, Section No. 542, Vol. 11, No. 288, Pg. 81,
September 17, 1987 (19870917)

ABSTRACT

PURPOSE: To prevent the destruction of an IC due to erroneous insertion by making the number of the power supply system pads of the **chip** same as the number of the rectangular electrodes of the package for **chip** carrier IC, and connecting the individual pads.

CONSTITUTION: The device comprises short rectangular electrodes 2 in contact with the circuit substrate or the socket for **chip** carrier IC, the same number of rectangular electrodes 3 as the number of the power supply system pads of a semiconductor **integrated circuit** to be encapsulated, and an insulating package 1 the **corners** of which were **cut** as usual. A semiconductor circuit **chip** 5 is mounted on this package, and the pads connected to the rectangular electrodes 3 corresponding to the power supply system pads are connected by means of bonding **wires**. As to the **rectangular** electrodes as the socket for **chip** carrier IC, if the socket is the one having electrodes in contact only the portions inherent to the rectangular shape, no power supply current flows even in the case of erroneous insertion of the semiconductor circuit device encapsulated in this package, preventing the destruction by a test.

30/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015961453

WPI Acc No: 2004-119294/200412

XRAM Acc No: C04-048005

XRFX Acc No: N04-095289

Integrated circuit, for wireless communication
systems, comprises circuit elements interconnected by secondary
conductor through vias at locations for coupling circuit elements
as alternative to primary **conductor**

Patent Assignee: JESSIE D (JESS-I); PERSICO C J (PERS-I)

Inventor: JESSIE D; PERSICO C J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030202331	A1	20031030	US 2002375510	P	20020424	200412 B
			US 2002192476	A	20020709	

Priority Applications (No Type Date): US 2002375510 P 20020424; US
2002192476 A 20020709

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030202331	A1	16	H05K-001/18	Provisional application	US 2002375510

Abstract (Basic): US 20030202331 A1

Abstract (Basic):

NOVELTY - An **integrated circuit** comprises **circuit elements** interconnected by a secondary **conductor** through vias at locations for coupling the circuit elements as an alternative to a primary **conductor**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating an **integrated circuit** to facilitate testing of interconnection of circuit elements prior to deposition of a low loss metal, comprising:

(a) forming a secondary **conductor** over a substrate to interconnect circuit elements as an alternative to a primary **conductor**; and

(b) forming vias at locations for coupling the second **conductor** to the primary **conductor** and the circuit elements.

USE - **Wireless communication** systems.

ADVANTAGE - The secondary **conductor** is formed using design guidelines such that it provides the required electrical **conductivity** when the primary **conductor** is not present but minimally interferes with the radio frequency performance of the primary **conductor**.

DESCRIPTION OF DRAWING(S) - The figure is a block diagram of a transceiver unit that may be used for **wireless communication**.

pp; 16 DwgNo 1/8

30/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015192509

WPI Acc No: 2003-253043/200325

XRPX Acc No: N03-201151

Antenna apparatus for use in non-contact type **integrated circuit card** reader/writer, has through-hole plating layers for connecting successive **coil pattern** layers to form single **coil pattern**

Patent Assignee: SHINKO DENKI KOGYO KK (SHIA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2003067682	A	20030307	JP 2001260400	A	20010829	200325 B

Priority Applications (No Type Date): JP 2001260400 A 20010829

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2003067682	A		5 G06K-017/00	

Abstract (Basic): JP 2003067682 A

Abstract (Basic):

NOVELTY - Multiple **conductor pattern layers** and resin insulators layer (11a) are alternately provided as multilayer structure and the successive **coil pattern** layers (10,10a-10d) are connected by through-hole plating layers (12) to form single **coil pattern**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for non-contact type **integrated circuit** reader/writer.

USE - In non-contact type **integrated circuit** reader/writer (claimed) for **communicating data** between non-contact type **integrated circuit (IC) card**.

ADVANTAGE - Increases communication distance without causing increase in size and components cost.

DESCRIPTION OF DRAWING(S) - The figure shows an explanatory view of the **coil pattern** of each layer of an antenna substrate.

(Drawing includes non-English language text).

coil pattern layers (10,10a-10d)
resin insulator layer (11a)
through-hole plating layer (12)
pp; 5 DwgNo 5/6

30/3,AB/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014593261

WPI Acc No: 2002-413965/200244

XRAM Acc No: C02-116947

XRPX Acc No: N02-325394

Pattern antenna for **wireless communication** devices, e.g. cellular phones, comprises inverted-F-shaped antenna pattern with feeding **conductor** patterns and grounding **conductor** patterns

Patent Assignee: SHARP KK (SHAF); MASUDA Y (MASU-I)

Inventor: MASUDA Y

Number of Countries: 004 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020024466	A1	20020228	US 2001927634	A	20010813	200244 B
DE 10142384	A1	20020321	DE 1042384	A	20010830	200244
JP 2002076735	A	20020315	JP 2000262724	A	20000831	200244
US 6404395	B1	20020611	US 2001927634	A	20010813	200244
CN 1341980	A	20020327	CN 2001132406	A	20010830	200247

Priority Applications (No Type Date): JP 2000262724 A 20000831

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020024466	A1		23	H01Q-001/00	
DE 10142384	A1			H01Q-001/38	
JP 2002076735	A		13	H01Q-001/38	
US 6404395	B1			H01Q-001/24	
CN 1341980	A			H01Q-013/08	

Abstract (Basic): US 20020024466 A1

Abstract (Basic):

NOVELTY - A pattern antenna has an inverted-F-shaped antenna pattern (1) comprises a feeding **conductor** pattern (1b) connected to a feeding transmission path (2) formed on a surface of a circuit board (4), and a grounding **conductor** pattern (1c) connected to a grounding **conductor** portion (3) formed on the surface of the circuit board.

DETAILED DESCRIPTION - INDEPENDENT CLAIM is also included for a **wireless communication** device comprising a pattern antenna that permits either transmission or reception of a communication signal to or from an external device.

USE - For **wireless communication** devices, e.g., cellular phones or indoor wireless local area network terminals.

ADVANTAGE - The invention is compact and light weight yet nevertheless permits wide-range transmission and reception, and to a **wireless communication** equipped with such a pattern antenna.

DESCRIPTION OF DRAWING(S) - The figure shows a plan view showing the configuration of the inverted-F-shaped antenna pattern.

Inverted-F-shaped antenna pattern (1)
Feeding **conductor** pattern (1b)
Grounding **conductor** pattern (1c)
Feeding transmission path (2)
Grounding **conductor** portion (3)
Circuit board (4)
pp; 23 DwgNo 1/22

30/3,AB/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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013301722

WPI Acc No: 2000-473657/200041

XRAM Acc No: C01-012087

XRFX Acc No: N01-030917

Manufacture of integrated inductor devices useful for impedance matching in radio frequency **integrated circuits** comprises filling a trench within a silicon substrate with porous silicon

Patent Assignee: KOREA ELECTRONICS & TELECOM RES INST (KOEL-N); ELECTRONICS & TELECOM RES INST (ELTE-N)

Inventor: PARK M; YOO H G; YU H K

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 99052173	A	19990705	KR 9771622	A	19971222	200041 B
US 6153489	A	20001128	US 98162784	A	19980930	200106
KR 281637	B	20010302	KR 9771622	A	19971222	200214

Priority Applications (No Type Date): KR 9771622 A 19971222

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 99052173	A			H01L-027/10	
US 6153489	A	14		H01L-021/20	
KR 281637	B			H01L-027/04	Previous Publ. patent KR 99052173

Abstract (Basic): US 6153489 A

Abstract (Basic):

NOVELTY - Integrated inductor devices are manufactured by forming a trench within the silicon substrate, filling a trench with a porous silicon by electroplating process using hydrofluoric acid-containing solvent as a pyrolysis solution to form a trench-shaped porous silicon layer, forming interlayer dielectric films on the resultant structure, and forming an upper **spiral** metal **pattern**.

DETAILED DESCRIPTION - Manufacture of integrated inductor devices on a silicon substrate comprises forming a trench within the silicon substrate (10), filling the trench with a porous silicon by electroplating process using hydrofluoric acid-containing solvent as a pyrolysis solution to form a trench-shaped porous silicon layer (19), forming a first interlayer dielectric film (12) on the resultant structure, depositing a lower metal line (13) on a portion of the first dielectric film, forming a second interlayer dielectric film (14) on the resultant structure, and forming an upper **spiral** metal **pattern** (16) having its central portion connecting with the lower metal line through a hole (15).

USE - For manufacturing inductor devices useful for impedance matching in the monolithic radio frequency **integrated circuits** for cellular phones, **wireless** modems, and other **communication** equipment.

ADVANTAGE - The method provides a high performance integrated inductors that have high quality factor, are capable of decreasing a parasitic capacitance of devices, and can minimize a mutual-coupling between the silicon substrate and metal levels.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a spiral inductor.

Silicon substrate (10)
First interlayer dielectric film (12)
Lower metal line (13)
Second interlayer dielectric film (14)
Hole (15)
Upper **spiral** metal **pattern** (16)
Porous silicon layer (19)
pp; 14 DwgNo 2B/5

30/3,AB/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX.
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011202922

WPI Acc No: 1997-180846/199717

XRPX Acc No: N97-148751

Transponder arrangement with antenna - has **conducting** surface and **coil** surface inclined at **angle** greater than 45 degrees relative to each another

Patent Assignee: LICENTIA PATENT-VERW GMBH (LICN); AEG

IDENTIFIKATIONSSYSTEME GMBH (AEGE); AEG IDENTIFIKATIONSSYSTEME (AEGE)

Inventor: BLOCH W; LEUCK L; MUELLER M; REITMAYER T; MILLER M

Number of Countries: 020 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19534229	A1	19970320	DE 1034229	A	19950915	199717 B
WO 9710520	A1	19970320	WO 96EP3980	A	19960911	199718
EP 850426	A1	19980701	EP 96931787	A	19960911	199830
			WO 96EP3980	A	19960911	
JP 11512519	W	19991026	WO 96EP3980	A	19960911	200002
			JP 97511654	A	19960911	
US 6249258	B1	20010619	WO 96EP3980	A	19960911	200137
			US 9843312	A	19980908	
EP 850426	B1	20020130	EP 96931787	A	19960911	200209
			WO 96EP3980	A	19960911	
DE 59608682	G	20020314	DE 508682	A	19960911	200220
			EP 96931787	A	19960911	
			WO 96EP3980	A	19960911	

Priority Applications (No Type Date): DE 1034229 A 19950915

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19534229	A1		5	H04B-001/59	
WO 9710520	A1	G	24	G01V-015/00	
Designated States (National): JP US					
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 850426	A1	G		G01V-015/00	Based on patent WO 9710520
Designated States (Regional): BE CH DE DK FI FR GB IT LI NL SE					
JP 11512519	W		21	G01S-013/75	Based on patent WO 9710520
US 6249258	B1			H01Q-007/08	Based on patent WO 9710520
EP 850426	B1	G		G01V-015/00	Based on patent WO 9710520
Designated States (Regional): BE CH DE DK FI FR GB IT LI NL SE					
DE 59608682	G			G01V-015/00	Based on patent EP 850426
Based on patent WO 9710520					

Abstract (Basic): DE 19534229 A

The arrangement has a transponder mounted on a metal surface (11). The transponder includes an antenna (A1) in the form of a flat air-cored choke, which is rectangular in shape. There is associated transponder electronic circuitry (E) connected to the antenna. The antenna and the electronics are preferably arranged on, or embedded in, a common carrier (T) that can be made from a plastic card.

The antenna is fastened, by adhesive, to the metal surface (M), and the angle between this surface and the surface of the carrier (W1) is 90 degrees. The distance between the choke and the metal surface is small, less than 20mm, and this surface can be coated in this area.

USE/ADVANTAGE - Suitable for data communications systems. Mechanically robust, easily portable and safe.

Dwg.1,2/5

30/3,AB/6 (Item 6 from file: 350).
 DIALOG(R)File 350:Derwent WPIX
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001481064

WPI Acc No: 1976-E3973X/197619

Arithmetic appts pulse shaper - delivers rectangular pulses with edges rigidly phase locked with input pulses

Patent Assignee: BLANK N B (BLAN-I)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
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Priority Applications (No Type Date): SU 1930335 A 19730601

Abstract (Basic): SU 474923 A

The invention relates to pulse engineering, and can be used in arithmetic devices, control devices for computers, and in **communication** lines in **data** input-output units. Its purpose is continuous control over wide limits of generated pulse width, realised by insertion of a potentiometer (5) into the collector circuit of a phase splitter (8) in the third logic circuit (3) whose output is connected to the fourth logic circuit. (4) supply wire. **Rectangular** pulses are applied to the logic circuit (2) input, inverted and applied to a multiple emitter transistor (7) in circuit (3); this transistor (7) becomes blocked, transistor (8) becomes **conducting** and capacitor (6) begins to charge; transistor (11) is blocked and circuit (3) output has high impedance; potential at the point (a) is determined by transistor (9), so that the capacitor (6) charging circuit time constant is varied, as internal resistance of transistor (9) is used as the **integrating circuit** resistor. A negative input pulse makes **conducting** transistor (11), through which capacitor (6) discharges.

33/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

5985373 INSPEC Abstract Number: B9809-1350H-034
Title: TFSOS: Quo vadis [SOS microwave devices]
Author(s): Lagnado, I.; De la Houssaye, P.
Author Affiliation: RDT&E Div., Naval Command Control & Ocean Surveillance Center, San Diego, CA, USA
Conference Title: Proceedings of the Eighth International Symposium on Silicon-on-Insulator Technology and Devices p.329-39
Editor(s): Cristoloveanu, S.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1997 Country of Publication: USA x+413 pp.
ISBN: 1 56677 176 5 Material Identity Number: XX98-00727
Conference Title: Proceedings of the Eighth International Symposium on Silicon-on-Insulator Technology and Devices
Conference Date: 31 Aug.-5 Sept. 1997 Conference Location: Paris, France

Language: English

Abstract: The ability to communicate anywhere, anytime is enabled by many technological factors. One of the most important is the integration of advanced analog radio frequency (RF) and microwave components (active and passive) with digital processors onto an affordable very large scale **integrated circuit** (VLSIC). These microwave **integrated circuits** (MICs) should provide for the same powerful reductions in cost that VLSI technology has achieved for digital applications. Further advances in technology will ultimately allow for the fabrication of a complete wireless transceiver to be placed on a single VLSI **chip**. The advances in the underlying silicon-on-insulator microwave device technology, particularly silicon-on-sapphire, will focus on the development of **wide bandwidth wireless communications** and ultimately the system-on-a-chip product.

Subfile: B

Copyright 1998, IEE

33/3,AB/2 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2004 ProQuest Info&Learning. All rts. reserv.

01510902 AAD9633766
THE INTEGRATION OF HIGH QUALITY FACTOR INDUCTORS ON MULTICHIP MODULE SILICON SUBSTRATES (**WIRELESS COMMUNICATION**)

Author: ZU, LONGQIANG

Degree: PH.D.

Year: 1996

Corporate Source/Institution: RUTGERS THE STATE UNIVERSITY OF NEW JERSEY
- NEW BRUNSWICK (0190)

Source: VOLUME 57/06-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3953. 145 PAGES

This dissertation addresses the design, simulation, fabrication and characterization of a novel RF inductor integrated on the multichip module (MCM) silicon substrate for **wireless communication** applications.

With today's fast expansion of **wireless communication**, **integrated circuits** are being driven to higher levels of integration by the consumer market for high density, enhanced functions, light weight, and small size devices. The integration of RF inductors on

MCM Si substrates provides a unique approach to the miniaturization of **integrated circuits**. Most importantly this approach allows the use of high-resistivity Si as the substrate for building high quality-factor inductors which have **wide** applications in **wireless communication** circuits such as filters, voltage controlled oscillators and matching networks.

High quality factor (Q) inductors have been designed and fabricated on high-resistivity (2000 $\Omega\text{-cm}$) Si substrates with MCM technology. Q-factors of 30 have been achieved for an inductor of 4 nH at 1 GHz. To enhance the Q-factor and reduce the parasitic coupling capacitance, a unique and novel design of a staggered double-metal-layered structure has been utilized by taking advantage of the double-layered metal lines in MCM. The variational method is used to identify the relative sensitivities of various device parameters in the characteristics of the RF inductors. It has been found that the quality factor is most sensitive to the spacing between adjacent metal wires in the inductor. The device process is fully compatible with MCM fabrication process, which uses polyimide and **aluminum** as the dielectric and metal layers, respectively. On-wafer S-parameter measurement techniques are used to characterize the fabricated inductors. An analytical method for the parameter extraction of the lumped element model is developed and for the first time a complete SPICE model of the RF inductor is obtained.

38/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

7149317 INSPEC Abstract Number: B2002-02-6250F-081

Title: Need wireless data? Think analog [CDPD]

Author(s): Webb, W.

Journal: EDN (US Edition) vol.46, no.26 p.43-6

Publisher: Cahnners Publishing,

Publication Date: 22 Nov. 2001 Country of Publication: USA

CODEN: EDNEFD ISSN: 0012-7515

SICI: 0012-7515(20011122)46:26L:43:NWDI;1-E

Material Identity Number: G340-2001-027

Language: English

Abstract: CDPD (cellular-digital-packet data), which operates over the nationwide analog cellular-phone system stands out as the most **widely** available **wireless-data-communications** protocol and is ideal for applications that require short bursts of data, such as e-mail, credit-card verification, vehicle location, dispatch, order entry, and inventory look-up. Many police departments also use CDPD to give officers on the street instant access to local and national criminal-justice information. CDPD shares radio-frequency channels with the AMPS (advanced- mobile-phone system), which has existed since 1983.

Subfile: B

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38/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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6033581 INSPEC Abstract Number: B9811-6210R-021, C9811-6130M-012

Title: MOMENTS-multimedia services in a narrow-bandwidth cellular environment

Author(s): Leisenberg, M.; Lindgren, T.

Author Affiliation: TELEMEDIA GmbH & Co. KG, Gutersloh, Germany

Conference Title: Multimedia Applications, Services and Techniques - ECMAST'98. Third European Conference. Proceedings p.246-59

Editor(s): Hutchison, D.; Schafer, R.

Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 1998 Country of Publication: Germany xvi+532 pp.

ISBN: 3 540 64594 2 Material Identity Number: XX98-01493

Conference Title: Multimedia Applications, Services and Techniques - ECMAST '98 Third European Conference Proceedings

Conference Date: 26-28 May 1998 Conference Location: Berlin, Germany

Language: English

Abstract: With the rapid success of the Internet and the World Wide Web online access to distributed multimedia data became feasible to experts, but also to regular customers of commercially available Internet services. At the same time relatively inexpensive and **widely** available **wireless data communication** services became available to the mass market. Within the coverage of cellular networks the vision of multimedia information access for "everyone, anytime, anywhere" become reality. This paper describes concept and implementation of MOMENTS (MOBile Media and ENTertainment Services)-a complete WWW on-line service for mobile customers. MOMENTS a joint project of 10 leading European companies. The project is partially funded by the European Union ACTS program. MOMENTS' client-server architecture employs cellular GSM/DCS-1800 telephone networks for data connection. MOMENTS provides several information services

specifically designed for mobile low-bandwidth applications, e.g.: automatically adapted third party on-line services Determination of customers geographical location. Dynamical provision of location dependent content. Dynamic SMS alert of events to be specified within the service, specifically processed and distributed Video/Audio material, variety of specific premium services especially designed for the mobile professional Enhanced animation/3D presentation techniques. Additionally, MOMENTS provides a unique micropayment, technology which employs the mobile phone SIM card for purse purposes. Charges for services are automatically deducted from this purse. The purse can be "filled" by on-line withdraw from the customers bank. The MOMENTS service also provides specific secure authentication capabilities. On clients site the usage of the system within a narrow-bandwidth environment is supported by a number of specifically designed browser plugins. Capabilities of plugins include audio/video decompression, visualization of vector data and VRML data, acquisition of mobile phone cell information. The complete system was successfully installed and tested on trial sites in Italy, UK, Germany.

Subfile: B C

Copyright 1998, IEE

38/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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5507881 INSPEC Abstract Number: B9704-6210L-020, C9704-5620L-006

Title: **Wireless** local and **wide** area network computing

Author(s): Angwin, A.J.

Author Affiliation: IBM UK Labs. Ltd., London, UK

Conference Title: IEE Colloquium on Wireless Technology (Digest No.1996/199) p.6/1-5

Publisher: IEE, London, UK

Publication Date: 1996 Country of Publication: UK 42 pp.

Material Identity Number: XX97-00069

Conference Title: IEE Colloquium on Wireless Technology (Digest No.1996/199)

Conference Sponsor: IEE

Conference Date: 14 Nov. 1996 Conference Location: London, UK

Language: English

Abstract: This paper briefly describes the current state of computing using **wireless** networking and **communications** both within the confines of a companies normal buildings or remotely from the confined environment. The development of small, lightweight and affordable portable computers has led to a demand for mobile communications from users. The advances in technology has led to PC card or PCMCIA modems and several types classes of wireless connectivity required by these users of the portable computers (notebooks, laptops, Personal Digital Assistants etc.) and the paper addresses these forms of connectivity, their use, strengths and how to integrate them into a business's information technology (IT) infrastructure. A strong parallel is emerging for **wireless data communications**, since the need for increased business efficiency and responsiveness requires near instant access to information wherever the user may be.

Subfile: B C

Copyright 1997, IEE

38/3,AB/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

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01526933 INSPEC Abstract Number: B80029574

Title: Module-to-module communication via fiber-optic piping

Author(s): Balliet, L.; Moore, V.S.; Romero, C.N.; Wantshouse, R.A.; Wylie, T.J.

Author Affiliation: IBM Corp., Armonk, NY, USA

Journal: IBM Technical Disclosure Bulletin vol.22, no.8B p.3519-20

Publication Date: Jan. 1980 Country of Publication: USA

CODEN: IBMTAA ISSN: 0018-8689

Language: English

Abstract: Metal land patterns on cards and wiring will transmit effectively serial digital pulses at high data rates. However, such data transmission rates (30-800 MHz) can cause interaction between land patterns and/or wires. In effect, the patterns are very effective antennas, and this causes problems such as random noise pickup. By the use of optical fibers, modules can be connected to one another and eliminate such noise/interference problems.

Subfile: B

38/3,AB/5 (Item 1 from file: 6)

DIALOG(R)File 6:NTIS

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2118257 NTIS Accession Number: TRI99-0004/XAB

Telecom and Network Security: Toll Fraud and Teleabuse Update

Telecommunications Reports International, Inc., Washington, DC.

Corp. Source Codes: 113571000

c1999 407p

Languages: English

Journal Announcement: GRAI9912

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NTIS Prices: PC\$265.00

Part I defines and summarizes the problem and its scope, familiarizing the reader with the new language used in this field, as well as detailing the costs of various types of fraud and how those costs have changed over recent years. Part II sets out toll fraud in wired services and equipment, including how fraud is committed and prevented in long distance, through the use of 800 numbers, PBX, calling cards, phone cards, automated attendant numbers, pay phones, electronic commerce and other means. Part III covers the fast-growing area of wireless services, including cloning, personal communications systems and satellites. Part IV deals with fraud that enters both wired and wireless services, through such vehicles as credit cards, calling and other phone cards, and prison toll fraud. Part V sets out interesting and informative case histories dealing with services as well as equipment. Part VI sets forth solutions and defenses, relates their success, and includes current laws and regulations, as well as proposed legislation and rules. Part VII defines and describes telabuse, particularly regarding improper employee use of email and the Internet, and offers solutions from corporations, universities and government agencies.

38/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:EI Compendex(R)
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04236225

E.I. No: EIP95082836572
Title: Setting the stage for wireless computing
Author: Zibrik, Larry
Corporate Source: Motorola Wireless Data Group
Source: IC Card Systems & Design v 5 n 6 Aug 1995. 4pp
Publication Year: 1995
CODEN: ICSDE3 ISSN: 1074-6269
Language: English

Abstract: Enabling a computing platform with **wireless communications** capability provides mobile connectivity. However, because computer systems and communications devices have been developed in isolation, their successful deployment for **wireless communications** is hindered. With this in mind, Motorola, in cooperation with computer industry partners, embarked on a wireless platform compatibility program to increase buyer confidence and market acceptance of wireless modem products. The program is designed to support the launch of PCMCIA **wireless wide area network service devices** into the marketplace. Although the program tests for wireless PC Card compatibility with leading portable computing system, it has the potential to form the basis of an industry-wide RF benchmark for all wireless PC Cards.

38/3,AB/7 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
(c) 2004 The HW Wilson Co. All rts. reserv.

2029102 H.W. WILSON RECORD NUMBER: BAST95042998
Take the risk out of **wireless communications**
Ruber, Peter;
Datamation v. 41 (July 15 1995) p. 35-6+
DOCUMENT TYPE: Feature Article ISSN: 0011-6963

ABSTRACT: Companies that utilize **wireless wide area data communications** should consider security measures for their networks. In particular, companies must guard against the use of a cellular device to access a server, the cloning of cellular phone serial numbers, and the pirating of wireless transmissions of sensitive data. To prevent unauthorized wireless access, companies should have reliable password protection. Moreover, they should switch from analog cellular carriers to digital cellular carriers and should use digital cellular phones/text pagers and digital PCMCIA fax modem **cards**. Finally, an extra layer of security can be added by using encryption software at the sending and receiving ends when transmitting sensitive data. A sidebar discusses the controversy surrounding encryption.

38/3,AB/8 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015598628

WPI Acc No: 2003-660783/200362
XRPX Acc No: N03-527069

Adaptive antenna **pattern control method in wireless**

communication network, involves creating null in receive antenna
pattern of wireless device at the location of unintended
source

Patent Assignee: STEADMAN K (STEA-I); WATERSTON J (WATE-I)

Inventor: STEADMAN K; WATERSTON J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030119558	A1	20030626	US 200128742	A	20011220	200362 B

Priority Applications (No Type Date): US 200128742 A 20011220

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030119558	A1	17	H04M-001/00	

Abstract (Basic): US 20030119558 A1

Abstract (Basic):

NOVELTY - An electromagnetic (EM) signal received over a packet switched **wireless communication** network by a communication device such as mobile telephone, is analyzed to determine whether the EM signal is from an intended or unintended source. A null is created in the received antenna pattern of the device is adapted at a location of the detected unintended source.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an apparatus for adaptively controlling antenna **pattern** of **wireless** network device.

USE - For adaptively controlling antenna **pattern** of **wireless communication** device such as mobile telephone, personal digital assistant (PDA), tablet-based computer, laptop computer, calculator, handheld gaming devices, picoradios and network **communication card** in **wireless** ad-hoc packet switched mobile network.

ADVANTAGE - Controls directionality of the antenna elements of the **wireless communication** device, appropriately and hence eliminates effects of interfering source, reduces bit error rates and improves signal quality.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart explaining the process of adaptive antenna pattern.

pp; 17 DwgNo 5/5

38/3,AB/9 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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014180743

WPI Acc No: 2002-001440/200201

Related WPI Acc No: 2001-543431

XRPX Acc No: N02-001075

Telesales and teleservicing system for gas, electricity and water companies, has router to establish video/voice communication link between central call center and POS station to transmit data in signal packets

Patent Assignee: AFS GROUP HOLDINGS LTD (AFSH-N)

Inventor: CAREY P; PAINE B D; WINTER D J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2360667	A	20010926	GB 20007253	A	20000324	200201 B

Priority Applications (No Type Date): GB 20007253 A 20000324

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
GB 2360667 A 11 H04L-012/56

Abstract (Basic): GB 2360667 A

Abstract (Basic):

NOVELTY - A router (13) establishes a video/voice communication link between a central call center (12) and a remotely located point of sale station (11) so as to transmit data in signal packets.

USE - For gas, electricity and water companies and for providing financial service such as mortgages, personal loans, life insurance, pensions, household and motor insurance, credit **cards** and catalogue based goods and services such as clothing, footwear, household goods and high value customer goods and inland revenue service through communication network such as public switch telephone network, integrated service digital network (ISDN), internet, local area network, **wide** area network (WAN), **wireless communication** network or an synchronous transfer mode (ATM) network.

ADVANTAGE - Since the transmitted information is encapsulated in signal packets, the information is allowed to be sent over multiple types or combinations of networks and hence a separate transmission protocol is not required for each different type of transmission media.

DESCRIPTION OF DRAWING(S) - The figure shows the diagrammatic representation of carrying out telesales and teleservicing.

Point of sale station (11)

Central call center (12)

Router (13)

pp; 11 DwgNo 1/1

38/3,AB/10 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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013838978

WPI Acc No: 2001-323190/200134

XRPX Acc No: N01-232757

IC module for **composite IC card**, has **wire**

to join electrode connection terminal and pad electrode of IC **chip**

Patent Assignee: TOPPAN PRINTING CO LTD (TOPP)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001084350	A	20010330	JP 99258570	A	19990913	200134 B

Priority Applications (No Type Date): JP 99258570 A 19990913

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
JP 2001084350 A 4 G06K-019/077

Abstract (Basic): JP 2001084350 A

Abstract (Basic):

NOVELTY - A vent is formed on the backside of the substrate (11) which has terminal electrodes (12a-12h) and IC mounting area (16) on its other side. Pad electrode of IC **chip** (21) and the electrode connecting terminal (14) are connected by a wire (31). Cream solder is embedded at the vent and the connection bump is formed on

substrate.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for compound IC card.

USE - For composite IC card used for both contact and non-contact data communication.

ADVANTAGE - Cost reduction of IC module is achieved, since manufacturing process is simplified and connection reliability is improved.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of IC module and IC card manufacturing method.

Substrate (11)

Terminal electrodes (12a-12h)

IC mounting area (16)

IC chip (21)

Wire (31)

pp; 4 DwgNo 3/3

38/3,AB/11 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012990929

WPI Acc No: 2000-162781/200015

XRPX Acc No: N00-121555

Radio integrated circuit card

Patent Assignee: TOSHIBA KK (TOKE); TOSHIBA COMMUNICATION TECHNOLOGY
(TOSH-N)

Inventor: KARASAWA J; SAITO Y; SEGAWA M

Number of Countries: 028 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 977145	A2	20000202	EP 99114633	A	19990726	200015 B
CN 1243294	A	20000202	CN 99111937	A	19990728	200025
JP 2000311226	A	20001107	JP 99213967	A	19990728	200061
KR 2000012026	A	20000225	KR 9930747	A	19990728	200102

Priority Applications (No Type Date): JP 9946392 A 19990224; JP 98212963 A 19980728; JP 98338934 A 19981130

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 977145	A2	E	43 G06K-019/077	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
LI LT LU LV MC MK NL PT RO SE SI

CN 1243294	A	G06K-019/07
JP 2000311226	A	28 G06K-019/07
KR 2000012026	A	G06K-019/077

Abstract (Basic): EP 977145 A2

Abstract (Basic):

NOVELTY - The IC card has at least two rectangular-spiral antennas (31,32) on module board (30), IC chip (23) has rectangular-spiral antenna (22) formed on insulating protection film (21) formed on chip surface. Semiconductor chip is mounted on board so antenna formed on it is opposite one of other two antennas.

DETAILED DESCRIPTION - IC card has antenna (22) on IC chip formed by bonding a piece of bonding wire among electrode pads on surface of IC chip. Antenna is formed of metallic film. A layer of antenna metallic film and a layer of

insulating film are laminated on surface of IC chip.

Antenna (31,32) are electrically connected to form closed loop.

INDEPENDENT CLAIMS are also included for a method of manufacturing a radio IC card, for a data reader/writer for the radio IC card, a radio tag and a method for manufacturing the radio tag.

USE - Radio IC card for data communication.

ADVANTAGE - Low cost as no need to use expensive mounting apparatus e.g. flip-chip bonder or wire-bonder, energy saving.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section view of the radio IC card.

Insulation protection film (21)

Rectangular-spiral antenna on chip (22)

IC chip (23)

Board rectangular-spiral antennas (31,32))

pp; 43 DwgNo 14/44

38/3,AB/12 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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012979875

WPI Acc No: 2000-151728/200014

XRPX Acc No: N00-112714

Wireless card reader-writer for data communication -

has phase switching device to control phase of signal supplied to antenna, corresponding to position of wireless card with respect to antenna

Patent Assignee: TOSHIBA KK (TOKE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000011107	A	20000114	JP 98178793	A	1998062	200014 B

Priority Applications (No Type Date): JP 98178793 A 19980625

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000011107	A		9 G06K-017/00	

Abstract (Basic): JP 2000011107 A

NOVELTY - When wireless card (30) is parallel to surface of antennas (15,18), signal supplied to the transmitting antenna is controlled to be in phase by phase switching device (16). The signal given to antennas is set to be in anti-phase, when wireless card is perpendicular to the transmitting antenna surface.

USE - Used for wireless data communication in object flow management, electronic commercial transaction and automatic gate opening and closing management.

ADVANTAGE - The bad influence due to directional variation of card, is reduced, hence practical usability is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the wireless card reader-writer. (15,18) Antennas; (16) Phase switching device; (30) Wireless card.

Dwg.1/11

38/3,AB/13 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

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07008854

CONTACTLESS IC CARD

PUB. NO.: 2001-236479 [JP 2001236479 A]
PUBLISHED: August 31, 2001 (20010831)
INVENTOR(s): AOKI HIROSHI
APPLICANT(s): MIYOTA KK
APPL. NO.: 2000-043846 [JP 200043846]
FILED: February 22, 2000 (20000222)

ABSTRACT

PROBLEM TO BE SOLVED: To prepare a contactless IC card capable of reduced man-hours, satisfactory in productivity and reduced cost.

SOLUTION: This contactless IC card has a flexible substrate, where a spiral antenna coil and a circuit pattern are formed and a circuit module formed by connecting an IC chip to the circuit pattern and sends and receives information to and from external equipment through the antenna coil, and a cut part is formed at the periphery of the inner peripheral side end part of the spiral antenna coil, formed on the flexible substrate and the inner peripheral side end part of the antenna coil is folded back together, with the flexible substrate from the cut part and connected to the circuit pattern provided on the outer peripheral side of the antenna coil.

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38/3,AB/14 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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05831080

SEMICONDUCTOR CARD AND PRODUCTION THEREOF

PUB. NO.: 10-114180 [JP 10114180 A]
PUBLISHED: May 06, 1998 (19980506)
INVENTOR(s): FUKAO RYUZO
KOHAMA KYOICHI
APPLICANT(s): HITACHI MAXELL LTD [000581] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-271924 [JP 96271924]
FILED: October 15, 1996 (19961015)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a highly reliable semiconductor card with a thin shape at a low cost by providing portions superimposed with a wire pattern formed on a substrate to be mounted with an IC chip with a covering lead line.

SOLUTION: A semiconductor card 1 with a non-contact type data transfer system comprises a PET film 2 to serve as the external casing film and the substrate to be mounted with parts, a print wire 3 to serve as a first wire pattern, a covering lead line 4 to serve as a second wire pattern, an IC chip 5, a coil 6 to serve as a non-contact data communication antenna, and a package member 7. In the production process, the first wire pattern 3 is formed with a silver paste by screen printing on the transparent PET substrate 2 placed on a glass plate 9, and the second wire pattern is

formed with the covering lead line 4 where the wires superimposed, with the lead line 4 and the wire pattern 3 junctioned with the silver paste. Then, the IC chip 5 and the coil 6 are mounted on the wire 3 so as to be junctioned.
? DS25-

40/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015148253

WPI Acc No: 2003-208780/200320

XRAM Acc No: C03-053020

XRPX Acc No: N03-166384

Composite semiconductor structure for wireless communication system, has monocrystalline semiconductor layer with antenna switch for switching RF signal between alternative communication paths

Patent Assignee: MOTOROLA INC (MOTI)

Inventor: HIGGINS R J; STENGEL R E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6462360	B1	20021008	US 2001921901	A	20010806	200320 B

Priority Applications (No Type Date): US 2001921901 A 20010806

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6462360	B1	36	H01L-021/28	

Abstract (Basic): US 6462360 B1

Abstract (Basic):

NOVELTY - A monocrystalline semiconductor layer formed on a monocrystalline perovskite oxide layer of a silicon substrate (110) as antenna switch for switching RF signal between the alternative communication paths.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) RF signal switching method; and
- (2) Input signal amplification method.

USE - E.g. **composite integrated circuit** for **wireless communication** system such as cellular phone.

ADVANTAGE - As the antenna switch has lower parasitic capacitance and low ON resistance, the power supply and ground connections are well protected and the harmful external signals are prevented from reaching the composite semiconductor structure. Electrical isolation is provided when electrical signals are applied to the composite semiconductor structure. Reduces the manufacturing cost of the semiconductor by using inexpensive high quality monocrystalline semiconductor layers, thereby improving yield and reliability.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor structure.

Silicon substrate (110)

pp; 36 DwgNo 27/44

43/3,AB/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

7360170 INSPEC Abstract Number: B2002-10-1350H-017, C2002-10-7410D-019

Title: Optimization of spiral inductor on silicon

Author(s): Alphones, A.; Wong Kai Yee

Author Affiliation: Sch. of Electr. & Electron. Eng., Nanyang Technol. Univ., Singapore, Singapore

Conference Title: 31st European Microwave Conference 2001. Conference Proceedings Part vol.1 p.129-32 vol.1

Publisher: Microwave Eng. Europe, London, UK

Publication Date: 2001 Country of Publication: UK 3 vol.(456+304+486)

pp.

Material Identity Number: XX-2001-01675

Conference Title: Proceedings of 31st European Microwave Conference

Conference Date: 24-28 Sept. 2001 Conference Location: London, UK

Language: English

Abstract: A simulation program is developed based on Grover's formulas and Greenhouse method to calculate the inductance value and Q-factor for particular dimension and width distribution of spiral inductors. This program changes the width distribution through a predetermined number of quadratic distributions in an attempt to reduce energy losses and improve Q-factor. The result of this program provides a higher Q-factor together with the possibility of reducing the overall dimension of square spiral inductors as compared with conventional designs. The coordinates of dimension for the simulated inductor are also calculated enabling ease of verification and fabrication. Finally, the calculated results are verified by simulating the inductor using HPADS momentum which is MOM based electromagnetic simulator. The ease of use and rapid results of this program can find its attractiveness in wireless communications and related areas.

Subfile: B C

48/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7285021 INSPEC Abstract Number: B2002-07-2575D-004, C2002-07-3240K-001
Title: Compact and low power consumed control circuit for wireless micromachine

Author(s): Tsuruta, K.; Mitsumoto, N.; Kawahara, N.; Shibata, T.; Sasaya, T.

Journal: Transactions of the Institute of Electrical Engineers of Japan, Part E vol.122-E, no.2 p.84-9

Publisher: Inst. Electr. Eng. Japan,

Publication Date: Feb. 2002 Country of Publication: Japan

CODEN: DGRF9 ISSN: 1341-8939

SICI: 1341-8939(200202)122/E:2L:84:CPCC;1-L

Material Identity Number: F143-2002-002

Language: Japanese

Abstract: We have developed a compact and low power consumed control circuit for a wireless in-pipe inspection micromachine. The micromachine consists of a CCD camera, a locomotive device, a system control circuit and wireless energy supply and communication devices, and moves in a 10 mm diameter pipe without wire and observes the inner surface of the pipe using the installed CCD camera. The developed control circuit controls all installed devices in the micromachine by commands from outside and transmits the image data from the CCD camera. As for the control circuit, the power consumption and the size are greatly restricted in order to be installed in the micromachine. In order to reduce the size of the circuit, we have newly developed an image data communication LSI based on a new architecture. The LSI has the size of 3.9 mm by 3.9 mm and the power consumption of 45 mW. To make the control circuit compact, we used a flip chip assembly for the LSI and eight more ICs in the system. Through a fabricated prototype of the micromachine, we have successfully confirmed the wireless in-pipe locomotion and wireless image data communication of 2.25 frames per second.

Subfile: B C

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DIALOG(R)File 2:INSPEC
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7139028 INSPEC Abstract Number: B2002-02-6250-005, C2002-02-3390C-020

Title: Wireless link system for communication and energy transmission of microrobot

Author(s): Mitumoto, N.; Tsuruta, K.; Shibata, T.; Kawahara, N.

Author Affiliation: Res. Labs., DENSO CORPORATION, Aichi, Japan

Conference Title: MHS2001. Proceedings of 2001 International Symposium on Micromechatronics and Human Science (Cat. No.01TH8583) p.57-62

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2001 Country of Publication: USA vii+222 pp.

ISBN: 0 7803 7190 9 Material Identity Number: XX-2001-02537

U.S. Copyright Clearance Center Code: 0-7803-7190-9/01/\$10.00

Conference Title: MHS2001. Proceedings of the 2001 International Symposium on Micromechatronics and Human Science

Conference Sponsor: City of Nagoya; Nagoya Urban Ind. Promotion Corp.; Chubu Ind. Advancement Center; Nagoya Univ.; Chubu Sci. & Technol. Center; Japan Soc. Mech. Eng.; Robotics Soc. Japan; Soc. Instrument & Control Eng.; IEEE Robotics & Autom. Soc.; Res. Committee on Micromechatronics; Tech.

Committee on Micro-mechanisms of Japan Soc. Precision Eng.; Chubu Bureau of Econ., Trade & Ind.; Micromachine Center; Federation of Micromachine Technol.; Aichi Prefecture; Mie Prefecture; Shizuoka Prefecture; Nagano Prefecture; Nagoya Chamber of Commerce & Ind.; Chubu Economic Federation; Nagoya Junior Chamber

Conference Date: 9-12 Sept. 2001 Conference Location: Nagoya, Japan

Language: English

Abstract: We have succeeded to develop a complete wireless link micromachine. It transmits image data and supplies energy without wire. It is done via microwave and light. The robot consists of a CCD camera, a locomotive device, a system control circuit and **wireless** energy supply and **communication** devices. The robot moves in a 10 mm **diameter** pipe without **wire** and observes the inner surface of the pipe using the installed CCD camera. We developed a compact control circuit which controls all the devices installed in the robot by commands from outside and transmits the image data from the CCD camera. An image **data communication** LSI based on a new architecture was developed. The LSI is based on the 0.35 μ m CMOS technology, and has the size of 3.9 mm by 3.9 mm. To make the control circuit compact, we used a flip **chip** assembly for the LSI and eight more ICs in the robot. Through a fabricated prototype of the microrobot, we have successfully confirmed the **wireless** image **data communication** of 2.27 frames per second and control of the robot by microwave technology.

Subfile: B C

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48/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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6894275 INSPEC Abstract Number: B2001-05-0170L-025, C2001-05-3355-007

Title: Control circuit in an in-pipe wireless micro inspection robot

Author(s): Tsuruta, K.; Sasaya, T.; Shibata, T.; Kawahara, N.

Author Affiliation: Res. Labs., Denso Corp., Aichi, Japan

Conference Title: MHS2000. Proceedings of 2000 International Symposium on Micromechatronics and Human Science (Cat. No.00TH8530) p.59-64

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2000 Country of Publication: USA .vii+247 pp.

ISBN: 0 7803 6498 8 Material Identity Number: XX-2001-00134

U.S. Copyright Clearance Center Code: 0 7803 6498 8/2000/\$10.00

Conference Title: MHS2000. Proceedings of 2000 International Symposium on Micromechatronics and Human Science

Conference Sponsor: IEEE Ind. Electron. Soc.; IEEE Robotics & Autom. Soc.; City of Nagoya; Nagoya Urban Ind. Promotion Corp.; Chubu Ind. Adv. Center; Nagoya Univ.; Chubu Sci. & Technol. Center; Japan Soc. Mech. Eng.; Robotics Soc. Japan; Soc. Instrum. & Control Eng.; Res. Committee on Micromechatronics; Tech. Committee on Micro-mechanisms of Japan Soc. of Japan Soc. Precision Eng.; Chubu Bureau of Int. Trade & Ind. MITI; Federation of Micromachine Technol.; Micromachine Center; Aichi Prefecture; Gifu Prefecture; Shizuoka Prefecture; Nagano Prefecture; Nagoya Chamber of Commerce & Ind.; Chubu Econ. Federation; Nagoya Junior Chamber

Conference Date: 22-25 Oct. 2000 Conference Location: Nagoya, Japan

Language: English

Abstract: We have been developing an in-pipe wireless micro robot for inspection on inner surface of pipes. The robot consists of a CCD camera, a locomotive device, a system control circuit and **wireless** energy supply and **communication** devices. The robot moves in a 10 mm **diameter** pipe without **wire** and observes the inner surface of the pipe using the installed CCD camera. We have developed a compact

control circuit which controls all the devices installed in the robot by commands from outside and transmits the image data from the CCD camera. As for the control circuit, the power consumption and the size are greatly restricted in order to be installed in the robot. In order to reduce the size of the circuit, we have newly developed an image **data communication** LSI based on a new architecture. The LSI is made of 0.35 μ m CMOS technology and has the size of 3.9 mm by 3.9 mm. To make the control circuit compact, we used a flip **chip** assembly for the LSI and eight more ICs in the robot. Through a fabricated prototype of the micro robot, we have successfully confirmed the **wireless image data communication** of 2.27 frames per second and control of the robot by microwave technology.

Subfile: B C

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48/3,AB/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

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6873368 INSPEC Abstract Number: B2001-04-6250B-017, C2001-04-5120-046

Title: Implementing a RAKE receiver for **wireless communications** on an FPGA-based computer system

Author(s): Shankiti, A.M.; Leeser, M.

Author Affiliation: SPS, Motorola Inc., Mansfield, MA, USA

Conference Title: FPGA'00. ACM/SIGDA International Symposium on Field Programmable Gate Arrays p.145-51

Publisher: ACM, New York, NY, USA

Publication Date: 2000 Country of Publication: USA vii+223 pp.

ISBN: 1 58113 193 3 Material Identity Number: XX-2000-00398

U.S. Copyright Clearance Center Code: 1 58113 193 3/2000/02...\$5.00

Conference Title: Proceedings of FPGA2000: ACM/SIGDA International Symposium on Field Programmable Gate Arrays

Conference Sponsor: ACM

Conference Date: 9-11 Feb. 2000 Conference Location: Monterey, CA, USA

Language: English

Abstract: RAKE receivers are **widely** used in the **wireless communications** industry. Currently, custom VLSI is the most popular implementation. Programmable and reconfigurable logic implementations are becoming more attractive because of their flexibility and due to technology advancements. We have implemented a RAKE receiver on an Annapolis Wildforce board with four Xilinx 4000 family **chips** for a total of 100000 gate equivalents. Our system is able to implement a RAKE receiver for underwater **data communication** systems that works in real time. We also investigate mapping a RAKE receiver to a Virtex **chip** for real-time atmospheric **wireless communication**.

Subfile: B C

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48/3,AB/5 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

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5361424 INSPEC Abstract Number: B9610-6220M-021, C9610-5260S-023

Title: CS-ACELP speech coding board and application systems

Author(s): Kaneko, T.; Kataoka, A.; Hayashi, S.; Moriya, T.

Author Affiliation: NTT Human Interface Labs., Japan

Journal: NTT Review vol.8, no.4...p.42-7

Publisher: NTT,

Publication Date: July 1996 Country of Publication: Japan

CODEN: NTTREK ISSN: 0915-2334

SICI: 0915-2334(199607)8:4L:42:ASCB;1-Z

Material Identity Number: N570-96004

Language: English

Abstract: The CS-ACELP program on a fixed-point DSP (digital signal processor) **chip** and the codec system with this **chip** were developed for the quality tests of the ITU (International Telecommunication Union) standardization. Using the DSP **chip**, a codec board for personal computers was also implemented to support the development of CS-ACELP application systems. The CS-ACELP algorithm, which is approved as a Speech Coding Draft Recommendation G.729 in the ITU, is expected to be used in the world-wide applications of personal **wireless communication** systems or the PHS (Personal Handy-phone System), time division multiplexing systems and, digital simultaneous voice and **data communications**.

Subfile: B C

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48/3,AB/6 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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02802444 JICST ACCESSION NUMBER: 96A0691588 FILE SEGMENT: JICST-E
ITU Standard Algorithm for 8-kbit/s Speech Coding. CS-ACELP Speech Coding
Board and Application Systems.

KANEKO T (1); KATAOKA A (1); HAYASHI S (1); MORIYA T (1)
(1) Nippon Telegr. and Teleph. Corp.

NTT Rev, 1996, VOL.8,NO.4, PAGE.42-47, FIG.9, TBL.3, REF.2

JOURNAL NUMBER: F0282BAW ISSN NO: 0915-2334

UNIVERSAL DECIMAL CLASSIFICATION: 621.395

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Commentary

MEDIA TYPE: Printed Publication

ABSTRACT: The CS-ACELP program on a fixed-point DSP(Digital Signal Processor) **chip** and the codec system with this **chip** were developed for the quality tests of the ITU(International Telecommunication Union) standardization. Using the DSP **chip**, a codec board for personal computers ~~was~~ also implemented to support the development of CS-ACELP application systems. The CS-ACELP algorithm, which is approved as a Speech Coding Draft Recommendation G. 729 in ITU, is expected to be used in the world-wide applications of personal **wireless communication** systems or PHS(Personal Handy-phone System), time division multiplexing systems and, digital simultaneous voice and **data communications**. (author abst.) ? DS 45-

53/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7864622 INSPEC Abstract Number: B2004-03-2575F-059

Title: Fabrication and evaluation of an on-chip micro-variable inductor

Author(s): Fukushige, T.; Yokoyama, Y.; Hata, S.; Masu, K.; Shimokohbe, A.

Author Affiliation: Precision & Intelligence Laboratory, Tokyo Inst. of Technol., Yokohama, Japan

Journal: Microelectronic Engineering Conference Title: Microelectron. English (Netherlands) vol.67-68 p.582-7

Publisher: Elsevier,

Publication Date: June 2003 Country of Publication: Netherlands

CODEN: MIENEF ISSN: 0167-9317

SICI: 0167-9317(200306)67/68L:582:FECM;1-5

Material Identity Number: F621-2003-005

U.S. Copyright Clearance Center Code: 0167-9317/2003/\$30.00

Conference Title: Micro- and Nano-Engineering 2002. 28th International Conference on Micro- and Nano-Engineering

Conference Date: 16-19 Sept. 2002 Conference Location: Lugano, Switzerland

Language: English

Abstract: Precise impedance matching in RF circuits and wide-range tuning on wireless communication equipment require variable inductors. We propose a new type of on-chip micro-variable inductor fabricated using MEMS technology. The inductor is a conical coil and has an inductance of a few nH. The coil height can be changed from zero to several hundred micrometers. The inductance value varies according to the height, which can be determined arbitrarily either at fabrication or after fabrication. Thin film metallic glass, a new MEMS material, was used to realize the conical coil. The measured and simulated electrical characteristics (S_{11} parameter) indicate that this inductor can be used at 50 MHz to 16 GHz. The relationship between the inductance and the height indicates that the tuning range of the inductance is 3.64 to 3.75 nH at 2 GHz.

Subfile: B

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53/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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7810384 INSPEC Abstract Number: B2004-01-6260F-037

Title: Electronic equalization in optical fiber communications

Author(s): Adali, T.; Wei Wang; Lima, A.O.

Author Affiliation: Dept. of Comput. Sci. & Electr. English, Maryland University, Baltimore, MD, USA

Conference Title: 2003 IEEE International Conference on Acoustics, Speech, and Signal Processing (Cat. No.03CH37404) Part vol.4 p. IV-497-500 vol.4

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2003 Country of Publication: USA 6 volume(xcviii+927+852+788+883+823+764) pp.

ISBN: 0 7803 7663 3 Material Identity Number: XX-2003-01651

U.S. Copyright Clearance Center Code: 0-7803-7663-3/03/\$17.00

Conference Title: Proceedings of International Conference on Acoustics, Speech and Signal Processing (ICASSP'03)

Conference Sponsor: IEEE Signal Process, Soc

Conference Date: 6-10 April 2003 Conference Location: Hong Kong, China

Language: English

Abstract: Electronic equalizers, which have been used widely in wireless and wireline communications, have recently been recognized as effective solutions for mitigating the impairments in the optical communications channel as well. Now with the increasing availability of voltage-tunable integrated circuits for high speed operation, equalizers, in particular those based on the minimum mean-square error (MMSE) criterion have emerged as practical and cost-effective solutions. Certain properties of the optical domain, however, are different than other communications systems where these equalizers have been used. We study the effects of these properties on the performance of the MMSE equalizers through eigenanalysis of the input autocorrelation matrix.

Subfile: B

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53/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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7797467 INSPEC Abstract Number: B2004-01-6135C-042, C2004-01-5260D-040

Title: Semiconductor IP core for ultra low power MPEG-4 video decode in system-on-silicon

Author(s): Dunlop, J.; Simpson, A.; Masud, S.; Wylie, M.; Cochrane, J.; Kinkead, R.

Author Affiliation: Amphion Semicond. Ltd., Belfast, UK

Conference Title: 2003 IEEE International Conference on Acoustics, Speech, and Signal Processing (Cat. No.03CH37404) Part vol.2 p. II-681-4 vol.2

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2003 Country of Publication: USA 6 volume(xcvi+927+852+788+883+823+764) pp.

ISBN: 0 7803 7663 3 Material Identity Number: XX-2003-00202

U.S. Copyright Clearance Center Code: 0-7803-7663-3/03/\$17.00

Conference Title: Proceedings of International Conference on Acoustics, Speech and Signal Processing (ICASSP'03)

Conference Sponsor: IEEE Signal Process, Soc

Conference Date: 6-10 April 2003 Conference Location: Hong Kong, China

Language: English

Abstract: An ultra low power, hardware accelerated architecture based semiconductor intellectual property core for MPEG-4 has been developed. This encompasses the simple profile of the video decoding algorithm. The core can provide motion picture quality video at up to CIF resolution. The implementation is based on the application of hardware acceleration of compute-intensive operations with an embedded RISC processor acting purely as a host controller. The architecture comprises custom hardware designs for lookup table decoders, bitstream parsing, discrete cosine transforms, motion compensation and colour space conversion. The hardware-software co-design approach results in high efficiency in both area and performance. The design has been validated on an FPGA-based development board with an LCD panel for visual demonstration of real-time decoded streaming video sequences. This MPEG-4 video decoder core has been ported to 130 nm ASIC technology using system-level integration techniques where the power dissipation is around 10 mWatts. The design is ideally suited to high-volume system-on-chip solutions for a wide range of wireless multimedia communication applications.

Subfile: B C

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53/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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7458943 INSPEC Abstract Number: B2003-01-6250-004
Title: Ka-band direct digital receiver
Author(s): Tatu, S.O.; Moldovan, E.; Brehm, G.; Ke Wu; Bosisio, R.G.
Author Affiliation: Dept.de Genie Electrique, Ecole Polytechnique de Montreal, Que., Canada
Journal: IEEE Transactions on Microwave Theory and Techniques vol.50, number11 p.2436-42
Publisher: IEEE,
Publication Date: Nov. 2002 Country of Publication: USA
CODEN: IETMAB ISSN: 0018-9480
SICI: 0018-9480(200211)50:11L:2436:BDDR;1-Y
Material Identity Number: I045-2002-013
U.S. Copyright Clearance Center Code: 0018-9480/02/\$17.00
Language: English
Abstract: A new direct-conversion wideband (26-28.5 GHz) six-port receiver is proposed for mass-market **wireless communications**. This six-port receiver is designed to operate without the need for precise power reading and the use of a digital signal processor that is usually required in other receivers. The proposed receiver architecture is chosen to satisfy requirements of hardware receivers used in high-speed QPSK communications. The receiver contains a receiver front-end, QPSK demodulator, and carrier recovery module. A reverse modulation loop was used to provide a rapid carrier recovery. The maximum bit rate is determined solely by the limiting speed of the baseband module. This new hardware receiver is proposed as a robust, rugged, low-cost receiver for use in **wide Ka-band wireless mass-market QPSK communications** such as local multipoint distribution system services, which is a prime example of communication equipment requiring such receivers. Bit-error-rate results are presented versus the noise and reference signal phase shift.
Subfile: B
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53/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC
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7325019 INSPEC Abstract Number: B2002-08-1350H-132
Title: Design and implementation of 40-GHz-band LNA MMICs with super low-gain flatness
Author(s): Woo-Jin Chang; Jin-Hee Lee; Hyung-Sup Yoon; Jae Yeob Shim; Kyung-Ho Lee
Author Affiliation: Dept. of Compound Semicond., Electron. & Telecommun. Res. Inst., Daejeon, South Korea
Journal: Journal of the Korean Physical Society Conference Title: J. Korean Phys. Society (South Korea) vol.40, no.4 p.552-6
Publisher: Korean Phys. Soc,
Publication Date: April 2002 Country of Publication: South Korea
CODEN: KPSJAS ISSN: 0374-4884
SICI: 0374-4884(200204)40:4L:552:DIBM;1-Z
Material Identity Number: J068-2002-007
Conference Title: 8th Korean Conference on Semiconductors

Conference Date: 14-15 Feb. 2001 Conference Location: Seoul, South Korea

Language: English

Abstract: This paper introduces the design and implementation of 40-GHz-band 4-stage/2-stage low-noise amplifiers with low-gain flatness for wide-band wireless multimedia and satellite communication systems. The 40-GHz-band 4-stage MMICs demonstrate a small signal gain of more than 20 dB, an input return loss of 10.2 dB, and an output return loss of 21.8 dB for 40~42 GHz. The gain flatness of the 40-GHz-band 4-stage LNA was 0.1 dB for 40~42 GHz. The noise figure of the 40 GHz-band 4-stage LNA was simulated to be less than 3.2 dB for 40~42 GHz. While the 40-GHz-band 2-stage LNA MMICs demonstrate a small signal gain of more than 10.5 dB, an input return loss of 8.6 dB, and an output return loss of 19.8 dB for 40~42 GHz. The gain flatness of the 40-GHz-band 2-stage LNA was 0.4 dB for 40~42 GHz. The noise figure of the 40-GHz-band 2-stage LNA was simulated to be less than 3.0 dB for 40~42 GHz. The chip size of the 2-stage and the 4-stage LNA MMICs were 2.1*1.7 mm/sup 2/ and 3.7*1.7 mm/sup 2/, respectively.

Subfile: B

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53/3,AB/6 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

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7301703 INSPEC Abstract Number: B2002-07-1350H-037

Title: Ka-band direct digital receiver using 0.25 mu m GaAs PHEMTs

Author(s): Ovidiu Tatu, S.; Moldovan, E.; Brehm, G.; Ke Wu; Bosisio, R.G.

Author Affiliation: Dept. de Genie Electr., Ecole Polytech. de Montreal, Que., Canada

Conference Title: 2002 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. Digest of Papers (Cat. No.02CH37280) p.155-8

Editor(s): Staudinger, J.

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2002 Country of Publication: USA xxxi+501 pp.

ISBN: 0 7803 7246 8 Material Identity Number: XX-2002-01590

U.S. Copyright Clearance Center Code: 0-7803-7246-8/02/\$10.00

Conference Title: Proceedings of 2002 IEEE Radio Frequency Integrated Circuits Symposium RFIC

Conference Sponsor: IEEE Microwave Theory and Techniques Society; IEEE Electron Devices Society; IEEE Solid States Circuits Soc

Conference Date: 2-4 June 2002 Conference Location: Seattle, WA, USA

Language: English

Abstract: A new direct conversion wideband (26 GHz - 28.5 GHz) six-port millimeter wave receiver using MMIC technology is proposed to meet the needs of mass-market wireless communications. This six-port receiver is designed to operate without the need for precise power reading and the use of digital signal processor (DSP) that is usually required in other receivers. The proposed receiver architecture is chosen to satisfy requirements of hardware receiver used in QPSK communications. The receiver contains one MMIC module consisting of a wide band six-port junction with four RF Schottky detectors, a receiver front-end and a base band module composed of video amplifiers and I&Q decoder. The maximum bit rate, at least 100 Mbs, is determined solely by the limiting speed of ancillary video amplifiers and analogue decoder. This new hardware receiver is proposed as a robust, rugged, low cost receiver for use in wide

Ka-band wireless mass market QPSK communications such as LMDS services that are a prime example of communication equipment requiring such receivers. BER results are presented in the presence of noise and local

oscillator (LO) phase shift.

Subfile: B

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53/3,AB/7 (Item 7 from file: 2)

DIALOG(R)File 2:INSPEC

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7231672 INSPEC Abstract Number: B2002-05-6250F-098

Title: Future directions and technology requirements of **wireless communications**

Author(s): Mochida, Y.; Takano, T.; Gambe, H.

Author Affiliation: Fujitsu Labs. Ltd., Kawasaki, Japan

Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224) p.1.3.1-8

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2001 Country of Publication: USA 951 pp.

ISBN: 0 7803 7050 3 Material Identity Number: XX-2002-00101

U.S. Copyright Clearance Center Code: 0-7803-7050-3/01/\$10.00

Conference Title: International Electron Devices Meeting. Technical Digest

Conference Sponsor: Electron Devices Society IEEE

Conference Date: 2-5 Dec. 2001 Conference Location: Washington, DC, USA

Language: English

Abstract: The third generation mobile services using W-CDMA first began in Japan. Further research on next mobile systems has already been started. The paper briefly describes the history of cellular systems and then introduces a technical outline of new generation systems. A broadband **wireless communication** requires a **wide** frequency bandwidth, huge delay spread tolerance, big transmission power and subscriber capacity. In order to obtain a smart solution, further digital processing approaches with the most advanced CMOS technology will be a key issue as well as the low-distortion and high-frequency power devices.

Subfile: B

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53/3,AB/8 (Item 8 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

7024065 INSPEC Abstract Number: B2001-10-6250-056

Title: A new direct millimeter wave six-port receiver

Author(s): Tatu, S.O.; Moldovan, E.; Ke Wu; Bosisio, R.G.

Author Affiliation: Dept. de Genie Electr. et Inf., Ecole Polytech. de Montreal, Montreal, Que., Canada

Conference Title: 2001 IEEE MTT-S International Microwave Symposium Digest (Cat. No.01CH37157) Part vol.3 p.1809-12 vol.3

Editor(s): Sigmon, B.

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2001 Country of Publication: USA 3 volume(lxiii+xxiv+xxiii+2262) pp.

ISBN: 0 7803 6538 0 Material Identity Number: XX-2001-01307

U.S. Copyright Clearance Center Code: 0 7803 6538 0/2001/\$10.00

Conference Title: 2001 IEEE MTT-S International Microwave Symposium Digest

Conference Date: 20-25 May 2001 Conference Location: Phoenix, AZ, USA

Language: English

Abstract: A new direct conversion wide band (23 GHz-31 GHz) six-port millimeter wave receiver suitable for **integrated circuit** fabrication is proposed to satisfy mass-market **wireless communications**. The receiver contains one multi chip module (MCM) consisting of a wide band six-port junction, four RF detectors (Schottky diodes), video amplifiers and I&Q decoder. The prototype circuits are fabricated in hybrid **integrated circuits**, and the receiver topology is suitable for fabrication in microwave monolithic **integrated circuits** (MMICs). This new hardware receiver is proposed as a robust, rugged, low cost receiver for use in wide band **wireless** mass market QPSK **communications**. Hand held and laptop terminals for future e-mail/multimedia services are a prime example of communication equipment needing such receivers. BER measurements and simulation results are presented in the presence of noise, adjacent signal interference, local oscillator (LO) phase shift and LO phase noise.

Subfile: B

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53/3,AB/9 (Item 9 from file: 2)

DIALOG(R)File 2:INSPEC

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6547174 INSPEC Abstract Number: B2000-05-1350H-017

Title: InGaP/GaAs provides high-linearity HBTs

Author(s): Browne, J.

Journal: Microwaves & RF vol.39, no.2 p.121-9

Publisher: Penton Publishing,

Publication Date: Feb. 2000 Country of Publication: USA

CODEN: MIRFDL ISSN: 0745-2993

SICI: 0745-2993(200002)39:2L:121:IGPH;1-2

Material Identity Number: D590-2000-005

U.S. Copyright Clearance Center Code: 0745-2993/2000/\$1.25+.60

Language: English

Abstract: Device technology has grown in leaps and bound over the last decade. Heterojunction-bipolar-transistor (HBT)-based RF **integrated circuits** (RF ICs) have gained **wide** acceptance among major **wireless** and broadband-**communications** equipment suppliers as the preferred technology for applications where high performance, high linearity, and competitive pricing are important. These RF IC products include power amplifiers (PAs) for cellular and personal-communications-services (PCS) handsets, driver amplifiers for cellular/PCS base stations, as well as cable-television (CATV)/fiber-cable line-driver amplifiers. In those applications, HBT-based products have overtaken many incumbent products based on gallium-arsenide (GaAs) metal-epitaxial-semiconductor field-effect transistor (MESFET) and silicon (Si) bipolar transistor technologies by providing high-performance, cost-effective solutions. The latest process advancement in HBT technology, indium-gallium-phosphide (InGaP) emitters on GaAs substrates, is the basis for a new Line of high-linearity gain blocks from Stanford Microdevices (Sunnyvale, CA) for applications to 8 GHz.

Subfile: B

Copyright 2000, IEE

53/3,AB/10 (Item 10 from file: 2)

DIALOG(R)File 2:INSPEC

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6416874 INSPEC Abstract Number: B2000-01-6250B-004, C2000-01-5620W-011

Title: An overview of UCSD's Center for Wireless Communications

Author(s): Acampora, A.S.

Author Affiliation: Center for Wireless Commun., California University, San Diego, La Jolla, CA, USA

Journal: IEEE Personal Communications vol.6, no.5 p.8-16

Publisher: IEEE,

Publication Date: Oct. 1999 Country of Publication: USA

CODEN: IPCME7 ISSN: 1070-9916

SICI: 1070-9916(199910)6:5L:8:OUCW;1-Q

Material Identity Number: B467-1999-006

U.S. Copyright Clearance Center Code: 1070-9916/99/\$10.00

Language: English

Abstract: UCSD's Center for Wireless Communications was founded in March 1995 as a partnership between the University and the wireless communications industry. Its goals include the definition and pursuit of a cutting-edge program of precompetitive, multidisciplinary research focused on wireless access systems, technologies, and applications; the creation of a relevant base of new knowledge with high commercial impact potential; and the production of graduates at all degree levels trained to meet industrial human resources needs. Of paramount importance to the achievement of these goals are the involvement, collaboration, and financial support of the CWCs industrial participants. Working in close cooperation with its industrial participants, the theme of broadband wireless access to the Internet was chosen as the unifying focus for the Center's programs, and five thrust areas have been defined: circuits, signal processing (smart antennas and compression), communication theory, networks, and software to wirelessly support multimedia applications. Seven specific goal-oriented projects are currently underway, each intended to meet the long-term interests of a subset of our industrial participants. These seven projects focus, respectively, on ad hoc home networks, universal wide-area wireless service, space-time processing, modulation/coding for enhanced coverage, linear power amplifiers, RF receivers, and changes to the Internet infrastructure needed to support ubiquitous broadband wireless access. Among the many issues being addressed are agent-based computing, division of responsibilities between the tetherless information portal and the infrastructure-based agents, battery-conserving protocols for the air interface, quality of service at the wireless networking layer, capacity enhancement and interference suppression on the radio air interface, modulation and coding, image and video compression, and low-power RF and integrated circuits for the handheld device.

Subfile: B C

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53/3,AB/11 (Item 11 from file: 2)

DIALOG(R)File 2:INSPEC

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5999087 INSPEC Abstract Number: B9809-1265F-072, C9809-5135-025

Title: An 800 MOPS 110 mW 1.5 V parallel DSP for mobile multimedia processing

Author(s): Igura, H.; Narita, S.; Naito, Y.; Kazama, K.; Kuroda, I.; Motomura, M.; Yamashina, M.

Author Affiliation: NEC Corp., Japan

Conference Title: 1998 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, ISSCC. First Edition (Cat. Number98CH36156) p.292-3

Editor(s): Wuorinen, J.H.

Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA 504 pp.
ISBN: 0 7803 4344,1 Material Identity Number: XX98-01042
U.S. Copyright Clearance Center Code: 0 7803 4344 1/98/\$10.00
Conference Title: 1998 IEEE International Solid-State Circuits
Conference. Digest of Technical Papers. ISSCC
Conference Sponsor: IEEE Solid-State Circuits Society; IEEE San Francisco
Sect.; Bay Area Council; University Pennsylvania
Conference Date: 5-7 Feb. 1998 Conference Location: San Francisco, CA,
USA

Language: English

Abstract: The central signal-processing unit for a portable multimedia terminal in the coming **wide-band wireless communication** age should meet the following three requirements: (1) high-performance for processing video-class wide-band digital signals, (2) low-power for extended battery life, (3) programmability to cope with applications with a small **chip** count. Conventional DSPs lack the high-performance, while emerging media processors consume too much power. This DSP exploits task-level, coarse-grained parallelism inherent in multimedia applications. This **chip** achieves performance in a power-efficient manner, while maintaining the programmability of conventional DSPs.

Subfile: B C

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53/3,AB/12 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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06720153

E.I. No: EIP04078018242

Title: VLSI design of a variable-length FFT/IFFT processor for OFDM-based communication systems

Author: Kuo, Jen-Chih; Wen, Ching-Hua; Lin, Chih-Hsiu; Wu, An-Yeu Andy

Corporate Source: Graduate Institute of Electron. English Department of Electrical Engineering National Taiwan University, Taipei 106, Taiwan

Source: Eurasip Journal on Applied Signal Processing v 2003 n 13 Dec 1 2003. p 1306-1316

Publication Year: 2003

CODEN: EJASCT ISSN: 1110-8657

Language: English

Abstract: The technique of orthogonal frequency division multiplexing (OFDM) is famous for its robustness against frequency-selective fading channel. This technique has been **widely** used in many **wired** and **wireless communication** systems. In general, the fast Fourier transform (FFT) and inverse FFT (IFFT) operations are used as the modulation/demodulation kernel in the OFDM systems, and the sizes of FFT/IFFT operations are varied in different applications of OFDM systems. In this paper, we design and implement a variable-length prototype FFT/IFFT processor to cover different specifications of OFDM applications. The cached-memory FFT architecture is our suggested VLSI system architecture to design the prototype FFT/IFFT processor for the consideration of low-power consumption. We also implement the twiddle factor butterfly processing element (PE) based on the coordinate rotation digital computer (CORDIC) algorithm, which avoids the use of conventional multiplication-and-accumulation unit, but evaluates the trigonometric functions using only add-and-shift operations. Finally, we implement a variable-length prototype FFT/IFFT processor with TSMC 0.35 μ m 1P4M CMOS technology. The simulations results show that the **chip** can perform (64,2048)-point FFT/IFFT operations up to 80 MHz operating frequency which

can meet the speed requirement of most OFDM standards such as WLAN, ADSL, VDSL (256 similar to 2K), DAB, and 2k-mode DVB. 21 Refs.

53/3,AB/13 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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06041795

E.I. No: EIP02166923873

Title: A 2-GHz down-converter with 3-dB bandwidth of 600 MHz using LO signal suppressing output buffer

Author: Watanabe, Osamu; Yamaji, Takafumi; Itakura, Tetsuro; Hattori, Ichiro

Corporate Source: Corp. Res. and Development Center Toshiba Corp., Kawasaki-shi 212-8582, Japan

Source: IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences v E85-A n 2 February 2002. p 286-292

Publication Year: 2002

CODEN: IFSEEX ISSN: 0916-8508

Language: English

Abstract: A 2-GHz down-converter for **wide-band wireless communication** systems is described. To achieve both wide-band output characteristic and LO signal suppression, an on-**chip** LC series resonator which is resonated at LO signal frequency and a transimpedance amplifier which is used in the output buffer circuit are used. To achieve a low sensitivity to temperature, two kinds of bias circuits; a V//T reference current source and a bandgap reference current source are used. The measured 3-dB bandwidth of 600MHz is achieved. The conversion gain varies less than 0.2dB within 200MHz plus or minus 10MHz and 400 MHz plus or minus 10 MHz band and 0.7 dB for the temperature range from -34 degree C to 85 degree C. At room temperature, conversion gain of 15 dB, NF of 9.5 dB and IIP3 of -5dBm are obtained respectively. The down-converter is fabricated using Si BiCMOS process with $f_{t}/f_{max}=20$ GHz, and it occupies approximately 1 mm*2. 5 Refs.

53/3,AB/14 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05944073

E.I. No: EIP01476740680

Title: Dielectric resonators raise your high-Q

Author: Fiedziuszko, S.J.; Holme, S.

Corporate Source: Space Systems LORAL, Palo Alto, CA, United States

Source: IEEE Microwave Magazine v 2 n 3 September 2001. p 50-60

Publication Year: 2001

CODEN: IEMMFF ISSN: 1527-3342

Language: English

Abstract: The applications of dielectric resonators in various microwave components are very cost effective and lead to significant miniaturization. Excellent performance in filters and oscillators is currently being achieved. Dielectric resonators are **widely** used in **wireless communication** systems. Additional applications include dielectric or superconductor testing and antenna applications, as well as radiating dielectric resonators. Miniature dielectric filled coaxial resonators are commonly used in wireless headsets. (Edited abstract) 39 Refs.

53/3,AB/15 (Item 4 from file: 8)
DIALOG(R)File 8:EI Compendex(R)
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05904895

E.I. No: EIP01416679633
Title: Wireless beyond the third generation - Facing the energy challenge
Author: Rabaey, J.M.
Corporate Source: BWRC EECS Department University of California,
Berkeley, CA, United States
Conference Title: International Symposium on Low Electronics and Design
(ISLPED'01)
Conference Location: Huntington Beach, CA, United States
Conference Date: 20010806-20010807
E.I. Conference Number: 58480
Source: Proceedings of the International Symposium on Low Power
Electronics and Design, Digest of Technical Papers 2001. p 1-3 (IEEE cat n
01TH8581)

Publication Year: 2001

Language: English

Abstract: After a stellar growth over the last decade driven by voice as
the killer app, **wireless communications** is now rapidly moving
into a new era propelled by data networking. For a **wide** host of
devices, **wireless** will serve as the "last interconnection hop" to
the high data rate wired networks. The basic trends in these devices can be
best summarized under the following two headers: "ubiquity" and "more
bits/sec". Both of these have some important ramifications on energy
dissipation. In this paper and accompanying presentation, we will outline
the predominant trends in wireless, analyze the energy challenge of those,
and examine a number of emerging solutions. 9 Refs.

53/3,AB/16 (Item 5 from file: 8)
DIALOG(R)File 8:EI Compendex(R)
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05837070

E.I. No: EIP01256548313
Title: High speed integrated optical wireless transceivers for
in-building optical LANs
Author: O'Brien, D.C.; Faulkner, G.E.; Jim, K.; Zyambo, E.B.; Edwards,
D.J.; Whitehead, M.; Stavrinou, P.; Parry, G.; Bellon, J.; Sibley, M.J.;
Lalithambika, V.A.; Joyner, V.M.; Samsudin, R.J.; Atkinson, R.; Holburn,
D.M.; Mears, R.J.
Corporate Source: Department of Engineering Science, Oxford, OX1 3PJ,
United Kingdom
Conference Title: Optical Wireless Communications III
Conference Location: Boston, MA, United States Conference Date:
20001106-20001107
E.I. Conference Number: 58118
Source: Proceedings of SPIE - The International Society for Optical
Engineering v 4214 2001. p 104-114
Publication Year: 2001
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: Maintaining high bandwidth indoor optical **wireless**
channels under a **wide** range of operating conditions usually requires
relatively complex transceiver components. Integrating optical,
optoelectronic and optical components using techniques that are suitable

for mass manufacture is an important step in the development of these systems. This paper describes work to develop low cost integrated tracking transmitter and receiver components for use in a cellular indoor optical wireless network. A seven channel demonstrator operating at 155Mb/s is under construction, using arrays of Resonant Cavity LEDs, PIN detectors, Silicon CMOS driver circuits and associated optics. Development of components, design methodology and initial results are detailed. 14 Refs.

53/3,AB/17 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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05639209

E.I. No: EIP00085291675

Title: Wide-band direct conversion receiver with on-chip A/D converters

Author: Parssinen, Aarno; Jussila, Jarkko; Ryyanen, Jussi; Sumanen, Lauri; Kivekas, Kalle; Halonen, Kari

Corporate Source: Helsinki Univ of Technology, Finl

Conference Title: 2000 Symposium on VLSI Circuits

Conference Location: Honolulu, HI, USA Conference Date: 19000615-19000617

E.I. Conference Number: 57181

Source: IEEE Symposium on VLSI Circuits, Digest of Technical Papers 2000. IEEE, Piscataway, NJ, USA. p 32-33

Publication Year: 2000

CODEN: 85PXA5

Language: English

Abstract: In **wireless communications**, the receiver architectures, which have on-chip channel selection filters like direct conversion or low-IF, are preferred to increase the integration level. Combining digital signal processing on the same **chip** with analog circuits would be desirable in the miniaturization. Some recent papers present highly integrated transceivers with mixed-mode or digital circuits on the same **chip** as left bracket 1 right bracket - left bracket 2 right bracket . However, only little discussion or experimental results have been given on the potential problems related to the system. This paper focuses on the design aspects of the single-chip direct conversion receivers, and gives experimental results of the BiCMOS prototype. The **chip** includes RF front-end, analog baseband signal processing and 6-bit A/D converters on the same die. It operates in the third generation **Wide-Band CDMA wireless** system at 2 GHz range.
(Author abstract) 3 Refs.

53/3,AB/18 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)
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04228001

E.I. No: EIP95082813852

Title: 2-V, 2-GHz low-power direct digital frequency synthesizer **chip** set for **wireless communication**

Author: Yamagishi, Akihiro; Ishikawa, Masayuki; Tsukahara, Tsuneo; Date, Shigeru

Corporate Source: NTT LSI Lab, Kanagawa, Jpn

Conference Title: Proceedings of the 1995 17th Annual Custom Integrated Circuits Conference

Conference Location: Santa Clara, CA, USA Conference Date:

19950501-19950504

E.I. Conference Number: 43410

Source: Proceedings of the Custom Integrated Circuits Conference. 1995.
IEEE, Piscataway, NJ, USA, 95CH35775. p 319-322

Publication Year: 1995

CODEN: PCICER ISSN: 0886-5930

Language: English

Abstract: A 2-GHz direct digital frequency synthesizer (DDFS) chip
-set that operates at the very low supply voltage of 2 V is introduced.
This microwave DDFS, the first to be fully implemented using LSI
technologies, consists of a CMOS DDFS-LSI with an internal 10-bit DAC and
Si-bipolar up-converters. To achieve both high purity and low power
dissipation, we use a distortion-free up-conversion architecture and an
efficient ROM output bit-width reduction technique. The synthesizer
achieves a wide spurious-free dynamic range of 53.7 dB and a low power
dissipation of less than 160 mW at 2 GHz. (Author abstract) 6 Refs.

53/3,AB/19 (Item 8 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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01356113

E.I. Monthly No: EI8306049001

E.I. Yearly No: EI83098322

Title: EVALUATION OF THE PARAMETERS OF MOTION OF AN OBJECT IN INDUCTIVE
COMMUNICATION SYSTEMS.

Author: Ivanov, V. S.; Ul'yanitskiy, Yu. D.

Source: Telecommunications and Radio Engineering (English translation of
Elektrosvyaz, and Radiotekhnika) v 36-37 n 3 Mar 1982 p 62-67

Publication Year: 1982

CODEN: TCREAG ISSN: 0040-2508

Language: ENGLISH

Abstract: Inductive communications (IC) or communication in the
induction zone, is widely used for wireless communication
inside organizations, for controlling the movement of transport facilities,
and for other purposes. The potential accuracy with which the parameters of
motion of an object can be measured in systems based on inductive
communication is determined. The optimal reception antenna geometry is
found when the object position and rate of displacement are measured
simultaneously. 4 refs.

53/3,AB/20 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

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10562022 Genuine Article#: 542AX Number of References: 5

Title: Design and implementation of 40-GHz-band LNA MMICs with super
low-gain flatness (ABSTRACT AVAILABLE)

Author(s): Chang WJ (REPRINT) ; Lee JH; Yoon HS; Shim JY; Lee KH

Corporate Source: Elect & Telecommun Res Inst, Dept Compound Semicond,
Microwave Devices Team, Taejon 305350//South Korea/ (REPRINT); Elect &
Telecommun Res Inst, Dept Compound Semicond, Microwave Devices
Team, Taejon 305350//South Korea/

Journal: JOURNAL OF THE KOREAN PHYSICAL SOCIETY, 2002, V40, N4 (APR), P
552-556

ISSN: 0374-4884 Publication date: 20020400

Publisher: KOREAN PHYSICAL SOC, 635-4, YUKSAM-DONG, KANGNAM-KU, SEOUL
135-703, SOUTH KOREA

Language: English Document Type: ARTICLE

Abstract: This paper introduces the design and implementation of 40-GHz-band 4-stage/2-stage low-noise amplifier with low-gain flatness for wide-band wireless multimedia and satellite communication systems. The 40-GHz-band 4-stage MMIC demonstrate a small signal gain of more than 20 dB, an input return loss of 10.2 dB, and an output return loss of 21.8 dB for 40similar to42 GHz. The gain flatness of the 40-GHz-band 4-stage LNA was 0.1 dB for 40similar to42 GHz. The noise figure of the 40 GHz-band 4-stage LNA was simulated to be less than 3.2 dB for 40similar to42 GHz. While the 40-GHz-band 2-stage LNA MMIC demonstrate a small signal gain of more than 10.5 dB, air input return loss of 8.6 dB, and an output return loss of 19.8 dB for 40similar to42 GHz. The gain flatness of the 40-GHz-band 2-stage LNA was 0.4 dB for 40similar to42 GHz. The noise figure of the 40-GHz-band 2-stage LNA was simulated to be less than 3.0 dB for 40similar to42 GHz. The chip size of the 2-stage and the 4-stage LNA MMICs were 2.1 x 1.7 mm(2) and 3.7x 1.7 mm(2), respectively.

53/3,AB/21 (Item 2 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

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10401809 Genuine Article#: 523JV Number of References: 5

Title: A 2-GHz down-converter with 3-dB bandwidth of 600 MHz using LO signal suppressing output buffer (ABSTRACT AVAILABLE)

Author(s): Watanabe S (REPRINT) ; Yamaji T; Itakura T; Hattori I

Corporate Source: Toshiba Co Ltd,Ctr Corp Res & Dev,Kawasaki/Kanagawa

2128582/Japan/ (REPRINT); Toshiba Co Ltd,Ctr Corp Res &

Dev,Kawasaki/Kanagawa 2128582/Japan/; Toshiba Co Ltd,Semicond

Co,Kawasaki/Kanagawa 2108520/Japan/

Journal: IEICE TRANSACTIONS ON FUNDAMENTALS OF ELECTRONICS COMMUNICATIONS AND COMPUTER SCIENCES, 2002, VE85A, N2 (FEB), P286-292

ISSN: 0916-8508 Publication date: 20020200

Publisher: IEICE-INST ELECTRONICS INFORMATION COMMUNICATIONS ENG,

KIKAI-SHINKO-KAIKAN BLDG MINATO-KU SHIBAKOEN 3 CHOME, TOKYO, 105, JAPAN

Language: English Document Type: ARTICLE

Abstract: A 2-GHz down-converter for wide-band wireless communication systems is described. To achieve both wide-band output characteristic and LO signal suppression, an oil-chip LC series resonator which is resonated at LO signal frequency and a transimpedance amplifier which is used in tile output buffer circuit are used. To achieve a low sensitivity to temperature, two kinds of bias circuits: a V-T reference current source and a bandgap reference current source are used. The measured 3-dB bandwidth of 600 MHz is achieved. The conversion gain varies less than 0.2 dB within 200 MHz +/- 10 MHz and 400 MHz +/- 10 MHz band and 0.7 dB for the temperature range from -34degreesC to 85degreesC. At room temperature. conversion gain of 15 dB. NF of 9.5 dB and IIP3 of -5 dBm are obtained respectively. The down-converter is fabricated using Si BiCMOS process with f(t) = 20 GHz, and it occupies approximately 1 mm(2).

53/3,AB/22 (Item 3 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

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09763539 Genuine Article#: 444VL Number of References: 24

Title: Space-time block-coded multiple access through frequency-selective fading channels (ABSTRACT AVAILABLE)

Author(s): Liu ZQ (REPRINT) ; Giannakis GB
Corporate Source: Univ Minnesota, Dept Elect & Comp
Engn, Minneapolis//MN/55455 (REPRINT); Univ Minnesota, Dept Elect & Comp
Engn, Minneapolis//MN/55455
Journal: IEEE TRANSACTIONS ON COMMUNICATIONS, 2001, V49, N6 (JUN), P
1033-1044

ISSN: 0090-6778 Publication date: 20010600
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST,
NEW YORK, NY 10017-2394 USA

Language: English Document Type: ARTICLE

Abstract: Mitigation of multipath fading effects and suppression of multiuser interference (MUI) constitute major challenges in the design of wide-band third-generation wireless mobile systems. Space-time (ST) coding offers an effective transmit-antenna diversity technique to combat fading, but most existing ST coding schemes assume flat fading channels that may not be valid for wide-band communications. Single-user ST coded orthogonal frequency-division multiplexing transmissions over frequency-selective channels suffer from finite-impulse response channel nulls (fades). Especially multiuser ST block-coded transmissions through (perhaps unknown) multipath present unique challenges in suppressing not only MUI but also intersymbol/chip interference. In this paper, we design ST multiuser transceivers suitable for coping with frequency-selective multipath channels (downlink or uplink). Relying on symbol blocking and a single-receive antenna, ST block codes are derived and MUI is eliminated without destroying the orthogonality of ST block codes. The system is shown capable of providing transmit diversity while guaranteeing symbol recovery in multiuser environments, regardless of unknown multipath. Unlike existing approaches, the mobile does not need to know the channel of other users. In addition to decoding simplicity, analytic evaluation and corroborating simulations reveal its flexibility and performance merits.

53/3,AB/23 (Item 4 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
(c) 2004 Inst for Sci Info. All rts. reserv.

08767408 Genuine Article#: 327LC Number of References: 16
Title: A new quasi-Yagi antenna for planar active antenna arrays (ABSTRACT AVAILABLE)

Author(s): Deal WR (REPRINT) ; Kaneda N; Sor J; Qian YX; Itoh T
Corporate Source: UNIV CALIF LOS ANGELES, DEPT ELECT ENGN/LOS ANGELES//CA/90095 (REPRINT)

Journal: IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, 2000, V48, N6 (JUN), P910-918

ISSN: 0018-9480 Publication date: 20000600
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST,
NEW YORK, NY 10017-2394

Language: English Document Type: ARTICLE

Abstract: In this paper, a novel broad-band planar antenna based on the classic Yagi-Uda dipole antenna is presented, and its usefulness as an array antenna is explored. This 'quasi-Yagi' antenna is realized on a high dielectric-constant substrate, and is completely compatible with microstrip circuitry and solid-state devices. This antenna achieves a measured 48% frequency bandwidth for voltage standing-wave ratio < 2, better than a 12-dB front-to-back ratio, smaller than -15 dB cross polarization, and 3-5-dBi absolute gain. Mutual coupling of the antenna in an array environment is investigated. Finally, three simple arrays are presented, demonstrating the usefulness of the antenna as an array

element. This novel antenna should find wide application in wireless communication systems, power combining, phased arrays, and active arrays, as well as millimeter-wave imaging arrays.

53/3,AB/24 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2004 ProQuest Info&Learning. All rts. reserv.

01839554 AADAAI3016714
Design techniques for low-power wide-band direct digital frequency synthesizers of spread spectrum communication applications
Author: Jiang, Jiandong
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: Iowa State University (0097)
Source: VOLUME 62/06-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 2867. 123 PAGES
ISBN: 0-493-27534-7

For frequency agile communication systems, fast frequency switching in fine frequency steps with good spectral purity is crucial. Direct Digital Frequency Synthesizer (DDFS) is best suitable for these applications, but is not widely employed in wireless communication systems due to its high power consumption. In general, low power and high integration design are two challenges for mixed signal-circuits and communication systems designers. In this dissertation, new design techniques for DDFS at both architecture and circuit levels are proposed and investigated in order to minimize power consumption and optimize performance. A ROM-less low power wide band DDFS prototype using segmented sine wave Digital-to-Analog Converter (DAC) were designed, fabricated and tested to demonstrate the new design techniques.

First, to further reduce power consumption and save chip area, two new phase interpolation ROM less DDFS architectures are proposed. Segmentation technique is applied to the design of sine wave DAC for DDFS: (1) based upon trigonometric identities, a segmented sine wave DAC with fine nonlinear interpolation DAC's is proposed; (2) based upon first order Taylor series and simple linear interpolation, a segmented sine wave DAC with a fine linear interpolation DAC is proposed. Second, a figure of merit (FM) is defined to find the optimal sine wave DAC segmentations for various resolutions of the segmented sine wave DAC's. The device mismatch effects on the performance of segmented sine wave were also discussed. Third, For DDFS using current-steering segmented sine wave DAC with 12-b phase resolution and 11-b amplitude resolution, a behavioral model in Verilog was used to verify the functionality and validate the architecture. Finally, a DDFS prototype was designed and fabricated in a standard 0.25 μ m CMOS process. The measured SFDR is better than 50 dB with output frequencies up to 3/8 of the 300 MHz clock frequency. The prototype occupies an active area of 1.4 mm² and consumes 240 mW for 300 MHz clock frequency. The new techniques reduce the power dissipation and die area substantially when compared to conventional ROM based DDFS designs with on-chip DAC.

53/3,AB/25 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2004 ProQuest Info&Learning. All rts. reserv.

01690293 AAD9918451
MIXED MATERIAL INTEGRATION FOR HIGH-SPEED APPLICATIONS (THIN FILM)

Author: KRISHNAMURTHY, NICOLE ANDREA

Degree: PH.D.

Year: 1998

Corporate Source/Institution; .GEORGIA INSTITUTE OF TECHNOLOGY (0078)

Source: VOLUME 60/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 768. 144 PAGES

A great demand for portable and highly integrated high speed electronic components and systems has recently surfaced as a result of the vast expansion of personal **communications** and other **wireless** applications. As more and more applications in personal communications require frequencies between 1 and 100 GHz, a reduction in the cost of III-V technology is necessary for a **wide** distribution of **wireless** products in the consumer market. III-V technology provides improved and unique functionality compared with silicon CMOS **integrated circuit** (IC) technology, yet current III-V technologies cannot meet all the demands of low cost, high levels of integration, low power, and performance because of high material costs and low yield compared with the current silicon technology.

In this thesis, thin film mixed material integration is investigated as a method to increase functionality at lower cost. InP active devices are removed from the growth substrate and integrated onto other host substrates such as silicon via substrate removal. Characterization of these devices is performed. Also, thin film passive components via deposition on free standing polyimide are evaluated for lower cost and increased design freedom. By optimizing the passives and III-V active components separately and then integrating the two opens a new realm in mixed material integration.

53/3,AB/26 (Item 1 from file: 94)

DIALOG(R)File 94:JICST-EPlus

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05496386 JICST ACCESSION NUMBER: 03A0547120 FILE SEGMENT: JICST-E

An 85-Mbit/s DQPSK MODEM-LSI Using a ROM Storage Capacity Reducing

Technique Based on Phase Plane Symmetry

YAMAGISHI AKIHIRO (1); TSUKAHARA TSUNEO (1); MURAGUCHI MASAHIRO (2)

(1) Ntt Maikuroshisutemuintegureshonken; (2) Nippon Telegraph and Telephone

Corp. (NTT), Photonics Laboratory, JPN

Denshi Joho Tsushin Gakkai Ronbunshi C, 2003, VOL.J86-C,NO.8, PAGE.845-852
, FIG.11, REF.6

JOURNAL NUMBER: S0623CAH ISSN NO: 1345-2827

UNIVERSAL DECIMAL CLASSIFICATION: 621.376 681.325/.326.009.16

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: On the phase detection method using ROM for construction of base band delay wave-detection circuit of phase modulation method **widely** used for **wireless communication** system, here was proposed a technique to reduce capacity of ROM using for phase detection by using phase plane symmetry. By using this technique, required ROM capacity can be reduced to its 1/5. By trial one- **chip** production of MODEM-LSI using 0.5 micron CMOS based on this technique, more than 85 Mbit/s of bandzone and 23 mA of low power at working of 80 Mbit/s were confirmed. And, by constructing DQPSK demodulation part using this LSI to carry out a folding test, 2dB of fixed deterioration at B.E.R. = $1e - 5$ could be obtained.

53/3,AB/27 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2004 Japan Science and Tech Corp(JST). All rts. reserv.

05186760 JICST ACCESSION NUMBER: 02A0490364 FILE SEGMENT: JICST-E
Voltage Controlled CMOS Phase-Shift Oscillator for Short-Range
Wireless Communication.

NAKAMURA MITSUO (1); MATSUOKA TOSHIMASA (1); TANIGUCHI KENJI (1)
(1) Osaka University, Graduate School of Engineering, JPN
Denshi Joho Tsushin Gakkai Ronbunshi C(Transactions of the Institute of
Electronics, Information and Communication Engineers C), 2002,
VOL.J85-C,NO.6, PAGE.449-454, FIG.13, REF.6

JOURNAL NUMBER: S0623CAH ISSN NO: 1345-2827

UNIVERSAL DECIMAL CLASSIFICATION: 621.373

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: Aiming at application of **chip-to-chip wireless communication** interface, and so on to short distance **wireless communication**, here was proposed a voltage controlled CMOS phase-shift oscillation circuit (VC CMOS PSOC) to output sinusoidal wave signal by a simple circuit construction. Oscillation frequency of a CMOS PSOC carried out trial production at 0.6 micron CMOS process, was about 600 MHz. In addition, as a result of tested on some items such as higher harmonic wave, tuning range of oscillation frequency, phase noise, and so on, it was found that VC CMOS PSOC could be used for short distance **wireless communication**, and that **wide** minituarization of the circuit scale could be realized.

53/3,AB/28 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2004 Japan Science and Tech Corp(JST). All rts. reserv.

05110263 JICST ACCESSION NUMBER: 02A0194968 FILE SEGMENT: JICST-E
Analog Circuit Techniques and Related Topics. A 2-GHz Down-Converter with
3-dB Bandwidth of 600 MHz Using LO Signal Suppressing Output Buffer.

WATANABE O (1); YAMAJI T (1); ITAKURA T (1); HATTORI I (2)

(1) Toshiba Corp., Kawasaki-shi, Jpn; (2) Toshiba Corp. Semiconductor Co.,
Kawasaki-shi, Jpn

IEICE Trans Fundam Electron Commun Comput Sci(Inst Electron Inf Commun Eng)
, 2002, VOL.E85-A,NO.2, PAGE.286-292, FIG.18, TBL.1, REF.5

JOURNAL NUMBER: F0699CAT ISSN NO: 0916-8508

UNIVERSAL DECIMAL CLASSIFICATION: 621.396 621.374.4

LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: A 2-GHz down-converter for **wide-band wireless communication** systems is described. To achieve both wide-band output characteristic and LO signal suppression, an on-**chip** LC series resonator which is resonated at LO signal frequency and a transimpedance amplifier which is used in the output buffer circuit are used. To achieve a low sensitivity to temperature, two kinds of bias circuits; a VT reference current source and a bandgap reference current source are used. The measured 3-dB bandwidth of 600 MHz is achieved. The conversion gain varies less than

0.2 dB within 200 MHz \pm 10 MHz and 400MHz \pm 10MHz band and 0.7dB for the temperature range from -34.DEG.C. to 85.DEG.C.. At room temperature, conversion gain of 15dB, NF of 9.5dB and IIP3 of -5dBm are obtained respectively. The down-converter is fabricated using Si BiCMOS process with $f_t=20$ GHz, and it occupies approximately 1 mm². (author abst.)

53/3,AB/29 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
(c) 2004 The HW Wilson Co. All rts. reserv.

1430872 H.W. WILSON RECORD NUMBER: BAST96069332
ASIC has functions for world-wide **wireless** standards
AUGMENTED TITLE: model TSC5000 from Texas Instruments Inc.
Kempainen, Stephen;
EDN v. 41 (Nov. 7 '96) p. 30
DOCUMENT TYPE: Product Evaluation ISSN: 0012-7515

ABSTRACT: The writer describes an application-specific **integrated circuit** that combines a digital signal processing core, a microcontroller core, RAM/ROM, and customizable logic to implement digital baseband functions for a variety of **wireless** standards. The **chip** from Texas Instruments, Dallas, Texas, is aimed at digital cellular phones, digital cordless phones, 2-way voice/data pagers, and other **wireless communications** applications.

53/3,AB/30 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2004 INIST/CNRS. All rts. reserv.

15988598 PASCAL Number: 03-0133535
WCDMA multiprocessor on **chip**: Design methodology using soft IP cores
Wireless and mobile **communications** II : Shanghai, 16-18 October 2002
GHALI K; HAMMAMI O
HEQUAN WU, ed; CHIH-LIN I, ed; VAARIO Jari, ed
ENSTA, 32 Bvd Victor, Paris, France
International Society for Optical Engineering, Bellingham WA, United States
Wireless and mobile communications. Conference, 2 (Shanghai CHN) 2002-10-16
Journal: SPIE proceedings series, 2002, 4911 120-128
Language: English
The implementation of the physical layer of W-CDMA on embedded devices requires optimizing the resources required due to the limited space and energy allowed. Although general purpose processors will eventually be embedded they are still lacking performance and more importantly they are not tailored to the computation requirements. We propose in this paper a methodology based on multiobjective genetic algorithms to tailor soft IP processor cores for the purpose of embedding W-CDMA.
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53/3,AB/31 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2004 INIST/CNRS. All rts. reserv.

14646700 PASCAL Number: 00-0318446

A GaAs MMIC chip set for 2 to 5 GHz fixed wireless services delivery

1999 IEEE wireless communications and networking conference :
New Orleans LA, 21-24 September 1999

BROWN D A; EDWARDS F M; JUPP P M; BIRKBECK J D; PENNINGTON D C; GREEN C R
; FORSTNER H P

Nortel Networks, Unknown; Roke Manor Research Limited, Unknown; Infineon Technologies, Unknown

IEEE. Communications Society, United States

WCNC '99 : wireless communications and networking conference (New Orleans LA USA) 1999-09-21

1999 727-731

Publisher: IEEE, Piscataway NJ

Language: English

The emergence of volume markets for fixed wireless delivery of telephony and data in the 2 to 5 GHz band drive the design of low cost integrated radio transceivers. The design of three GaAs MMICs for the implementation of a 3.5 GHz radio front-end is described, which together with catalogue available silicon integrated circuits forms the radio part of a residential transceiver for fixed wireless service delivery. The three low cost plastic packaged GaAs chips constitute a receive down-converter, transmit up-converter and +31.6 dBm power amplifier. The application of this GaAs chip set to broadband (data) wireless access is also considered.

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53/3,AB/32 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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016011553

WPI Acc No: 2004-169404/200416

XRPX Acc No: N04-135105

World-wide-walkie-talkie for wireless communication,
has solar recharging sub system to recharge batteries using light
source/power from sun, and push-to-talk external function buttons to
execute built-in software program

Patent Assignee: MCZEAL A (MCZE-I)

Inventor: MCZEAL A

Number of Countries: 099 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200414050	A1	20040212	WO 2002US36947	A	20021115	200416 B

Priority Applications (No Type Date): US 2002210480 A 20020731

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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WO 200414050	A1	E 189	H04M-001/00	
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Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA
CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN
IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ
OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA
ZM ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB
GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

Abstract (Basic): WO 200414050 A1

Abstract (Basic):

NOVELTY - The talkie (60, 61) has a solar recharging sub system that recharges batteries by using a light source or power from the sun. A push-to-talk and talk-internet external function buttons execute a built-in software program stored on a microchip **integrated circuit** board. The push-to-talk button has a unit that initiates and establishes instant communications sessions between telephones, computers, and the Internet (54).

DETAILED DESCRIPTION - A net2phone or compatible internet based voice over Internet protocol (VoIP) and network system of servers provide high quality of service (Qos) voice calls, voice chat, Internet protocol facsimile calls and manages user and communication sessions between the public switched telephone network, any data network or the internet. The talk-internet external function button has a unit that initiates the computer to computer voice calls or voice over Internet protocol telephone calls to any telephone, computer, or Internet device via any data network, the public switched telephone network, or the internet.

USE - Used for **wireless communication**.

ADVANTAGE - The solar recharging sub system automatically recharges the batteries by using a light source or power from the sun. The talkie establishes instant low cost and real time global communications to the public switched telephone network via a data network e.g. Internet. The push-to-talk button triggers instant communication between devices connected to the Internet or the public switched telephone network, thus allowing the walkie-talkie to instantly communicate with the computer based internet users or any telephone, fax machine, or computer connected to the world wide telephone network.

DESCRIPTION OF DRAWING(S) - The drawing shows a generalized view of a network structure and a wide area data network together with a voice over Internet protocol (VoIP) secured server.

Internet (54)

Registered user database (58)

World-wide-walkie-talkies (60, 61)

Internet protocol (IP) phone (102)

pp; 189 DwgNo 11/41

53/3,AB/33 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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015682433

WPI Acc No: 2003-744622/200370

Related WPI Acc No: 2003-787181

XRPX Acc No: N03-596382

Radio frequency transceiver **integrated circuit** for **wireless communication**, has local oscillator that adjusts uncompensated local oscillation signal based on frequency correction, to produce RF oscillation signal

Patent Assignee: BROADCOM CORP (BROA-N); BEHZAD A R (BEHZ-I); ROFOUGARAN A (ROFO-I); SHI Z (SHIZ-I)

Inventor: BEHZAD A; ROFOUGARAN A; SHI Z; BEHZAD A R

Number of Countries: 032 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030138034	A1	20030724	US 200252870	A	20020118	200370 B
			US 2002255378	A	20020926	
EP 1330043	A2	20030723	EP 20031134	A	20030120	200370

EP 1330044 A2 20030723 EP 20031135 A 20030120 200370

Priority Applications (No Type Date): US 2002255378 A 20020926; US
200252870 A 20020118; US 2002274655 A 20021021; US 2003340419 A 20030110

Patent Details:

Patent No Kind Lan' Pg Main IPC Filing Notes

US 20030138034 A1 24 H04B-001/38 CIP of application US 200252870

EP 1330043 A2 E H04B-001/40

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

EP 1330044 A2 E H04B-001/40

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): US 20030138034 A1

Abstract (Basic):

NOVELTY - The transceiver has a local oscillator (316) with frequency correction unit (304B) that adjust uncompensated local oscillation signal based on frequency correction to produce RF local oscillation signal. The receiver (304A) and transmitter (304C) of transceiver respectively down converts incoming RF signal into baseband signal and up converts outgoing baseband signal into RF signal based on RF oscillation signal.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for RF signal down converting method.

USE - For up converting and down converting signals used in wide hand wireless communication systems using communication devices such as cellular telephone, two way radio, personal digital assistant, personal computer, laptop computer, home entertainment equipment.

ADVANTAGE - The down conversion and up conversion of the signals are performed efficiently and the effects of the frequency drift are eliminated without the need for converting the RF signals to intermediate frequency signal and without the use of large, expensive and heavy SAW filters for signal processing.

DESCRIPTION OF DRAWING(S) - The figure shows the functional schematic diagram of the direct conversion RF transceiver.

radio circuitry (304)

receiver (304A)

frequency conversion unit (304B)

transmitter (304C)

baseband processing circuitry (308)

low noise amplifiers (312)

mixers (316)

pp; 24 DwgNo 9/13

53/3,AB/34 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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015068514

WPI Acc No: 2003-129030/200312

XRPX Acc No: N03-102594

Wireless transmission system for spread spectrum based communication system, varies information bit spreading factor based on distance between transmitter and receiver, and transmission path characteristics

Patent Assignee: SONY CORP (SONY); IWASAKI (IWAS-I); SUGAYA S (SUGA-I)

Inventor: IWASAKI J; SUGAYA S

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020172262	A1	20021121	US 2002138100	A	20020502	200312 B
JP 2002335228	A	20021122	JP 2001137828	A	20010508	200312
JP 2003110531	A	20030411	JP 2001303012	A	20010928	200334

Priority Applications (No Type Date): JP 2001303012 A 20010928; JP 2001137828 A 20010508

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20020172262	A1	36	H04B-001/69	
JP 2002335228	A	11	H04J-013/00	
JP 2003110531	A	17	H04J-013/00	

Abstract (Basic): US 20020172262 A1

Abstract (Basic):

NOVELTY - The ultra-wide spread spectrum based **wireless** transmission system has information bit spreading factor varied depending on the distance of linkage between a transmitter (36) and a receiver, or depending on the transmission path characteristics.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) **Wireless communication** system;
- (2) Wireless transmission apparatus;
- (3) Wireless reception apparatus;
- (4) Wireless transmission method;
- (5) **Wireless communication** method;
- (6) Wireless reception method;
- (7) Information bits spread process implementing program; and
- (8) Information bits de-spread process implementing program.

USE - Used in spread spectrum type **wireless communication** system.

ADVANTAGE - Enables to switch appropriately between the use of low-speed information bit and high-speed information bit while retaining the spread code **chip** rate and hence provides a transmission method which meets the system scalability and which effectively utilizes the wireless transmission path.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the wireless transmission unit.

Transmitter (36)
pp; 36 DwgNo 3/25

53/3,AB/35 (Item 4 from file: 350).
DIALOG(R)File 350:Derwent WPIX
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013989699

WPI Acc No: 2001-473913/200151

Structure of synchronous **wide** band cdma for **wireless** packet **communication**

Patent Assignee: KOREA ELECTRONICS & TELECOM RES INST (KOEL-N)

Inventor: AHN D H; HAN G C; KIM M T; OH H S

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2001010279	A	20010205	KR 9929078	A	19990719	200151 B
KR 347529	B	20020803	KR 9929078	A	19990719	200309

Priority Applications (No Type Date): KR 9929078 A 19990719

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001010279	A		1	H04B-001/69	
KR 347529	B			H04B-001/69	Previous Publ. patent KR 2001010279

Abstract (Basic): KR 2001010279 A

Abstract (Basic):

NOVELTY - A structure of a synchronous **wide** band CDMA for **wireless** packet **communication** is provided to be applicable to packet communication as well as circuit communication with improving demodulation efficiency of a receiver.

DETAILED DESCRIPTION - An IF band pass filter(102) filters only wide band including information in the output signals of a mixer(101). A QPSK demodulator(103) receives the signal outputted from the IF band pass filter(102) for generating carrier wave signal having same phase and orthogonal phase on the basis of the first IF clock signal generated in a PLL block(105), and separates I channel and Q channel by using the carrier wave signal. An A/D converter(104) converts an analog base band signal into a digital sample. The PLL block(105) generates a master clock which becomes a clock source for operation of a modem. A TCXO(Temperature Controlled Crystal Oscillator)(106) supplies a reference clock to the PLL block(105) and varies the reference clock according to the output value of a low pass filter(107). A match filter block(108) receives a digital sample and calculates an energy by **chip** units, and compares the ~~calculated~~ energy with an inner set energy. A synchronous code tracking block(109) receives a digital sample, detects a timing error by **chip** unit, and controls timing by sub-**chip** units for meeting code synchronization and generating a PN **chip** clock. A channel phase and frequency error tracking block(110) separates only a pilot signal from the received signal and calculates amplitude and composition of the channel. A synchronous demodulating block(11) demodulates the QPSK modulated signal by traffic channels for restoring a symbol.

pp; 1 DwgNo 1/10

58/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

00078543 INSPEC Abstract Number: B70000473

Title: Electrical interconnection of ~~micromodule~~ circuit devices

Assignee(s): Philco-Ford Corp

Patent Number: US 3429788 Issue Date: 690225

Application Date: 660408

Priority Appl. Number: US 541219

Country of Publication: USA

Language: English

Abstract: A method for making electrical connections to the terminal wires of **integrated circuit** devices, comprising the steps of: providing such devices with terminal wires extending from at least one side thereof; plating said wires with a metal capable of being removed by a suitable etchant; assembling a plurality of said devices so that terminal wires extend substantially unidirectionally; encapsulating the assembly in an electrically insulative material having interspersed therein particles of a material capable of being dissolved by the etchant, to form a body having terminal wires protruding therefrom; smoothing the side of the insulative block encapsulating the protruding terminal wires so that the terminal wires and the **metal plated** thereon are exposed in cross-section, and to expose portions of the embedded particles at the smooth surface; etching the exposed ~~particles~~ and portions of the recited plated metal; and electrically interconnecting the exposed terminal wire portions by applying the desired interconnection pattern upon the etched side of the insulative block and across the exposed portions of the terminal wires. The method characterized in that said last recited step comprises; plating a layer of metal upon the etched side of said insulative block and upon the exposed portions of the terminal wires; depositing on said layer of **metal** an etch **resist** defining the desired terminal **wire** interconnection **pattern** ; and etching away the exposed portions of the layer of metal to form the desired interconnection pattern. The method further characterized in that plating said layer of metal comprises the steps of depositing a first layer of metal on the etched side of said block by **electroless plating** techniques followed by depositing a second layer of metal on the first layer of metal by **electroplating** techniques.

Subfile: B

61/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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6535961 INSPEC Abstract Number: B2000-04-2140-012

Title: Microfabricated toroidal-type planar inductors for MEMS and power electronic applications

Author(s): Liakopoulos, T.M.; Ahn, C.H.

Author Affiliation: Center for Microelectron. Sensors & MEMS, Cincinnati University, OH, USA

Conference Title: Proceedings of the Fifth International Symposium on Magnetic Materials, Processes, and Devices Applications to Storage and Microelectromechanical Systems (MEMS) p.402-12

Editor(s): Romankiw, L.T.; Krongelb, S.; Ahn, C.H.

Publisher: Electrochem. Soc, Pennington, NJ, USA

Publication Date: 1999 Country of Publication: USA xv+706 pp.

ISBN: 1 56677 214 1 Material Identity Number: XX-1999-02008

Conference Title: Proceedings of the Fifth International Symposium on Magnetic Materials, Processes, and Devices Applications to Storage and Microelectromechanical Systems (MEMS)

Conference Date: 1-6 Nov. 1998 Conference Location: Boston, MA, USA

Language: English

Abstract: This paper describes new microfabricated toroidal-type planar inductors with different types of magnetic cores for MEMS and power electronic applications. In order to fabricate these multi-layer three dimensional inductive components, a new UV-LIGA lithography process for thick photoresist was developed. The fabricated coils consist of a rectangular-shaped permalloy electroplated magnetic core parallel to the wafer and electroplated copper conductor lines that form the winding around the core. These micromachined inductors are 4 mm*1.5 mm*150 mu m and feature a high Q factor, low resistance values (~1 Omega), and inductance values as high as 14 mu H. The optional introduction of an air gap in the magnetic core can affect the electromagnetic properties of these devices at low and high frequencies. These inductive components are fabricated with a CMOS compatible process and can be integrated with power electronic circuits for applications such as an on-chip DC/DC power converter.

Subfile: B

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61/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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6102961 INSPEC Abstract Number: B9901-0170J-096

Title: Integrated solenoid-type inductors for high frequency applications and their characteristics

Author(s): Young-Jun Kim; Allen, M.G.

Author Affiliation: Core Technol. Res. Center, Samsung Semicond., San Jose, CA, USA

Conference Title: 1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No.98CH36206) p.1247-52

Publisher: IEEE, New York, NY, USA

Publication Date: 1998 Country of Publication: USA xxv+1476 pp.

ISBN: 0 7803 4526 6 Material Identity Number: XX98-01334

U.S. Copyright Clearance Center Code: 0 7803 4526 6/98/\$10.00

Conference Title: 1998 Proceedings. 48th Electronic Components and Technology Conference (Cat. No.98CH36206)

Conference Sponsor: IEEE Components, Packaging & Manufacture Technol. Society;

Electron. Ind. Assoc

Conference Date: 25-28 May 1998 Conference Location: Seattle, WA, USA

Language: English

Abstract: New solenoid-type integrated inductors for high frequency applications have been realized using a surface micromachining technique and a polymer sacrificial layer, and their geometrical characteristics have been investigated. In general, integrated inductors can suffer from low Q factors and/or self-resonant frequencies when compared to their discrete counterparts. A spiral-type inductor, one of the dominant choices as an integrated inductor, requires relatively large two-dimensional spaces. In addition, the direction of flux of the **spiral** type inductor is **perpendicular** to the substrate, which can cause more interference with underlying **circuitry** or other **integrated** passives in a vertically stacked multi-**chip** module (MCM). The proposed inductor in this research has an air core to reduce unwanted stray capacitance that can be added due to a magnetic core, and **electroplated copper** coil to reduce the series resistance. An important feature of the proposed inductor geometry is introducing an air gap between the substrate and the **conductor** coil in order to reduce the effects of the substrate dielectric constant. This air gap can be realized using a polyimide sacrificial layer and a surface micromachining technique. Therefore, the resulting inductor can have less substrate-dependent magnetic properties, less stray capacitance, and higher Q-factor. Inductors with different geometrical aspects, such as air gap height, core size, and number of turns, have been designed and fabricated on ceramic substrates. A variational study of these **inductors** has been performed to assess the impact of the geometrical aspects on the inductor performance at high frequency. The measured inductance of these inductors varies from 2nH to 20 nH, and maximum Q-factor 10-60.

Subfile: B

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61/3,AB/3 (Item 1 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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06060663

E.I. No: EIP02226960062

Title: Contact **conductivity** detection in poly(methyl methacrylate)-based microfluidic devices for analysis of mono- and polyanionic molecules

Author: Galloway, Michelle; Stryjewski, Wieslaw; Henry, Alyssa; Ford, Sean M.; Llopis, Shawn; McCarley, Robin L.; Soper, Steven A.

Corporate Source: Department of Chemistry Louisiana State University, Baton Rouge, LA 70803-1804, United States

Source: Analytical Chemistry v 74 n 10 May 15 2002. p 2407-2415

Publication Year: 2002

CODEN: ANCHAM ISSN: 0003-2700

Language: English

Abstract: An on-column contact **conductivity** detector was developed for the analysis of various mono- and polyanionic compounds separated by electrophoresis **chips** fabricated in poly(methyl methacrylate) (PMMA) using hot embossing techniques from **Ni electroforms**. The detector consisted of a pair of Pt **wires** (127 μ m **diameter**) with an end-to-end spacing of approximately 20 μ m and situated within the fluidic channel. The waveform applied to the electrode pair was a bipolar pulse with a frequency of 5.0 kHz and was used to reduce the charging current from measurement so that the current recorded at the end of one pulse is more representative of the solution **conductivity**. Using the

detector, separations of amino acids, peptides, proteins, and oligonucleotides were demonstrated. For the amino acids and peptides, free-solution zone electrophoresis was performed. A calibration plot for the amino acid alanine was found to be linear from approximately 10 to 100 nM in a carrier electrolyte consisting of 10 mM triethylammonium acetate. The concentration detection limit was found to be 8.0 nM, with the corresponding mass detection limit equal to 3.4 amol (injection volume = 425 pL). The protein separations with **conductivity** detection were performed using MEKC, in which the carrier electrolyte contained the anionic surfactant sodium dodecyl sulfate (SDS) above its cmc. Near baseline resolution was achieved in the PMMA microchip for a solution containing 8 different proteins. In the case of the DNA fragments, capillary electrochromatography was used with a C18-modified PMMA **chip** and a carrier electrolyte containing an ion-pairing agent. 59 Refs.

61/3,AB/4 (Item 2 from file: 8)
DIALOG(R)File 8:EI Compendex(R)
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05089402

E.I. No: EIP98084333173

Title: Integrated solenoid-type inductors for high frequency applications and their characteristics

Author: Kim, Yong-Jun; Allen, Mark G.,

Corporate Source: Samsung Electronics Co, Ltd, Kyungki-Do, South Korea

Conference Title: Proceedings of the 1998 48th Electronic Components & Technology Conference

Conference Location: Seattle, WA, USA Conference Date: 19980525-19980528

E.I. Conference Number: 48782

Source: Proceedings - Electronic Components and Technology Conference 1998. IEEE, Piscataway, NJ, USA, 98CB36206. p 1247-1252

Publication Year: 1998

CODEN: PECCA7 ISSN: 0569-5503

Language: English

Abstract: New solenoid-type integrated inductors for high frequency applications have been realized using a surface micromachining technique and a polymer sacrificial layer, and their geometrical characteristics have been investigated. In general, integrated inductors can suffer from low Q factors and/or self-resonant frequencies when compared to their discrete counterparts. A spiral-type inductor, one of the dominant choices as an integrated inductor, requires relatively large two-dimensional spaces. In addition, the direction of flux of the **spiral** type inductor is **perpendicular** to the substrate, which can cause more interference with underlying **circuitry** or other **integrated** passives in a vertically stacked multi-**chip** modules (MCM). The proposed inductor in this research has an air core to reduce unwanted stray capacitance that can be added due to a magnetic core, and **electroplated copper** coil to reduce the series resistance. An important feature of the proposed inductor geometry is introducing an air gap between the substrate and the **conductor** coil in order to reduce the effects of the substrate dielectric constant. This air gap can be realized using a polyimide sacrificial layer and a surface micromachining technique. Therefore, the resulting inductor can have less substrate-dependent magnetic properties, less stray capacitance, and higher Q-factor. Inductors with different geometrical aspects, such as air gap height, core size, and number of turns, have been designed and fabricated on ceramic substrates. A variational study of these inductors has been performed to assess the

impact of the geometrical aspects to the inductor performance at high frequency. The measured inductance of these inductors varies from 2 nH to 20 nH, and maximum Q-factor 10-60. (Author abstract) 6 Refs.

61/3,AB/5 (Item 1 from file: 305)
DIALOG(R)File 305:Analytical Abstracts
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351858 AA Accession Number: 65-09-F-10155 DOC. TYPE: Journal
Contact **conductivity** detection in poly(methyl methacrylate)-based microfluidic devices for analysis of mono-and polyanionic molecules.
AUTHOR: Galloway, M. ; Stryjewski, W. ; Henry, A. ; Ford, S. M. ; Llopis, S. ; McCarley, R. L. ; Soper, S. A.*
CORPORATE SOURCE: Dept. Chem., Louisiana State Univ., Baton Rouge, LA 70803-1804, USA
JOURNAL: Anal. Chem., (Analytical Chemistry), Volume: 74, Issue: 10, Page(s): 2407-2415
CODEN: ANCHAM ISSN: 0003-2700
PUBLICATION DATE: 15 May 2002 (20020515) LANGUAGE: English
ABSTRACT: An on-column contact **conductivity** detector was developed for the analysis of various mono-and polyanionic compounds separated by electrophoresis **chips** fabricated in poly(methyl methacrylate) (PMMA) using hot embossing techniques from **Ni electroforms**. The detector consisted of a pair of Pt **wires** (127 μ m diameter) with an end-to-end spacing of approximately 20 μ m and situated within the fluidic channel. The waveform applied to the electrode pair was a bipolar pulse with a frequency of 5.0 kHz and was used to reduce the charging current from measurement so that the current recorded at the end of one pulse is more representative of the solution **conductivity**. Using the detector, separations of amino-acids, peptides, proteins, and oligonucleotides were demonstrated. For the amino-acids and peptides, free-solution zone electrophoresis was performed. A calibration plot for the amino acid alanine was found to be linear from approximately 10 to 100nM in a carrier electrolyte consisting of 10mM-triethylammonium acetate. The concentration detection limit was found to be 8.0nM, with the corresponding mass detection limit equal to 3.4 amol (injection volume = 425 pl). The protein separations with **conductivity** detection were performed using MEKC, in which the carrier electrolyte contained the anionic surfactant SDS above its **critical** micelle concentration. Near baseline resolution was achieved in the PMMA microchip for a solution containing 8 different proteins. In the case of the DNA fragments, capillary electrochromatography was used with a C18-modified PMMA **chip** and a carrier electrolyte containing an ion-pairing agent.

61/3,AB/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015996363
WPI Acc No: 2004-154213/200415
XRAM Acc No: C04-061212
XRPX Acc No: N04-123238

Smaller-size semiconductor device comprises printed circuit board mounted with semiconductor **chip** and metallic **wires** that connect

conductive patterns with metallic plated layers on the electrodes formed on the **chip**

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID); EGAWA Y (EGAW-I); UCHIDA Y (UCHI-I)

Inventor: EGAWA Y; UCHIDA Y

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030132516	A1	20030717	US 2003341463	A	20030114	200415 B
JP 2003209218	A	20030725	JP 20026786	A	20020115	200415

Priority Applications (No Type Date): JP 20026786 A 20020115

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030132516	A1		18	H01L-021/44	
JP 2003209218	A		17	H01L-025/065	

Abstract (Basic): US 20030132516 A1

Abstract (Basic):

NOVELTY - A smaller-size semiconductor device comprises semiconductor **chip** (12, 14) has circuitry and is mounted on a printed circuit board (10) having **conductive patterns** (22). Electrodes (16) are formed on periphery of main surface of the **chip**. Metallic plated layers are formed on the electrodes of the **chip**. Metallic wires (18, 24) are electrically connecting the respective **conductive patterns** with the metallic plated layers on electrodes.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing a semiconductor device comprising preparing a printed circuit board, forming a metallic plated layer on the electrodes in a lump by **electroless plating**, mounting the semiconductor **chip** on the printed circuit board, and connecting the electrodes with the **conductive patterns** respectively by metallic wires.

USE - For use as high functional semiconductor device.

ADVANTAGE - The device has high connecting reliability, and is designed at lower cost. The first electrode of the device has decreased diameter, and can be easily arranged and disposed in a less area.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the semiconductor device.

Printed circuit board (10)

Semiconductor **chip** (12, 14)

Electrodes (16)

Metallic wires (18, 24)

Metallic plated layers (20a, 20b)

Conductive patterns (22)

Solder balls (23)

pp; 18 DwgNo 3A/16

61/3,AB/7 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

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05374669

CHIP TYPE COIL AND ITS MANUFACTURE

PUB. NO.: 08-330169 [JP 8330169 A]

PUBLISHED: December 13, 1996 (19961213)

INVENTOR(s): OKUYAMA SHINGO

ARISHIRO MASATOSHI

APPLICANT(s): MURATA MFG CO LTD [000623] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-137602 [JP 95137602]
FILED: June 05, 1995 (19950605)

ABSTRACT

PURPOSE: To reduce the cost by providing the coil **conductor** with a plating **film** formed by wet plating.

CONSTITUTION: An electric insulation layer 8 are formed on an electric insulating substrate 2 while covering a coil **conductor** 3 and a jump **conductor** 6. The substrate 2 is provided, at the opposite ends, with a pair of terminal electrodes 9, 10. The coil **conductor** 3 is connected electrically, at one end 4, with one terminal electrode 9 and, at the other end 5, with the other terminal electrode 10 through the jump **conductor** 6. The coil **conductor** 3 is obtained by forming a plating film of silver, gold or **copper** high **conductivity** by wet plating, e.g. **electroplating** or **electroless plating**, on the substrate 2 and then **patterning** the plating film **spirally**.

61/3,AB/8 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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05081288

ELECTROFORMING METHOD FOR STAMPER FOR MANUFACTURING OPTICAL RECORDING MEDIUM

PUB. NO.: 08-036788 [JP 8036788 A]
PUBLISHED: February 06, 1996 (19960206)
INVENTOR(s): HIROBE FUMITAKE
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-172483 [JP 94172483]
FILED: July 25, 1994 (19940725)

ABSTRACT

PURPOSE: To control the thickness of a metal film adhered to the outer periphery immediately and continuously and to make the thickness of the metal film uniform by altering the region to be put outside from **electroforming** liquid surface when **electroforming** of glass original disk is carried out while putting out a part of the outer periphery of the disk from the liquid surface of **electroforming**.

CONSTITUTION: After glass original disk 1 is spin-coated with photoresist, it is pattern- exposed by a laser exposing unit, developed, uneven **pattern** of **concentric** circles is formed, **nickel** is then sputtered by a **nickel chip** 3, and a part of the outer periphery of the glass original disk treated to be **conductive** by the sputtering is put outside from the liquid surface of **electroforming** liquid 2 of **electroforming**. The region put outside is dried at the end when it is put outside half or more when it is rotated at 20-30rpm to be **electroformed**. Then, the region put outside is set to 20% or less of the entire disk 1. The thickness distribution of the plate of the **electroformed** film is varied according to the state of the liquid 2, but since the plate thickness distribution of the film can be immediately and continuously changed by regulating the region to be put outside from the liquid 2 surface, the plate thickness control is facilitated.

61/3,AB/9 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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02327762
PREPARATION OF THERMAL HEAD

PUB. NO.: 62-244662 [JP 62244662 A]
PUBLISHED: October 26, 1987 (19871026)
INVENTOR(s): SAIDA KATSUAKI
MOTOYOSHI YUKIO
APPLICANT(s): SEIKO INSTR & ELECTRONICS LTD [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-087647 [JP 8687647]
FILED: April 16, 1986 (19860416)
JOURNAL: Section: M, Section Number 684, Volume 12, Number 116, Pg. 119, April 13, 1988 (19880413)

ABSTRACT

PURPOSE: To obtain a thermal head used in the output part of a facsimile or a printer, by electrically connecting a first **conductor** pattern formed on a substrate to the second **conductor** pattern capable of being led to the outside of the substrate by a short pattern being the same resistor film as a heat generator and, formed simultaneously with the heat generator and applying **electroplating** treatment to the surface of the first **conductor** pattern.

CONSTITUTION: A resistor film 6 having to become a heat generator is formed to the entire surface of a glazed substrate 5, and a heat generator 7 and a short pattern 8 are formed simultaneously. Next, a **conductor** film 9, for example, consisting of lower layer **chromium** and upper layer **copper** each having a thickness of several hundred nm is formed to the entire surface of the substrate 5 and a current supply **conductor** pattern 10 to the heat generator, a common pattern 11, a data transmitting **pattern** 12 and signal **wires** 13 for guiding the timing signal of the power source wiring or switching of drive IC from the outside are formed. Thereafter, a protective layer is formed to the heat generator part and a resist is further formed to a plating unnecessary part to cover the same, and common A and common B are connected to a plating power source, and **nickel** plating and gold plating are continuously formed to the exposed part of each **conductor** pattern at every 1 μ m thickness to cut off the common B becoming unnecessary.

61/3,AB/10 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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01557043
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 60-035543 [JP 60035543 A]
PUBLISHED: February 23, 1985 (19850223)
INVENTOR(s): OOTA YUTAKA
KOBAYASHI HARUFUMI
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-143693 [JP 83143693]

FILED: August 08, 1983 (19830808)
JOURNAL: Section: E, Section Number 325, Volume 09, Number 154, Pg. 145, June
28, 1985 (19850628)

ABSTRACT

PURPOSE: To enable the electrical connection of a back surface of the element with a metallic **conductor layer** by a method wherein after the metallic **conductor layer** on a surface of an organic insulating film substrate in an element mounting region is removed, said organic insulating film of substrate in this region is removed to the metallic **conductor** on the back surface so as to form a recess and the element is mounted in this recess.

CONSTITUTION: A glass epoxy substrate whose both surfaces are covered with Cu is prepared and a through hole 13 is opened on the desired position of said substrate. After that, the overall plating is performed by **electroless plating** thereby **coating** the inner wall of the through hole 13 with a Cu layer 12. Next, the desired Cu pattern 12'' is formed by photolithography and etching techniques on the both surfaces of the glass epoxy substrate. The Cu layer on a front surface is removed whereas the Cu layer on a back surface is left. Next, the glass epoxy of substrate in a dice mounting region is removed to the thin Cu layer on the back surface so as to form a recess 14. Next, the surface of the Cu pattern 12'' is coated with an Ni -Au plating **layer** to form a **conductor** pattern 15, after which a dice 16 is mounted in the recess 14 and electrodes are connected to the **conductor pattern** 15 by a **wire** 17.

61/3,AB/11 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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01443561

WIRE FOR BONDING OF SEMICONDUCTOR ELEMENT

PUB. NO.: 59-155161 [JP 59155161 A]
PUBLISHED: September 04, 1984 (19840904)
INVENTOR(s): YORITA YOICHI
APPLICANT(s): DAIICHI DENKO KK [416661] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-030041 [JP 8330041]
FILED: February 23, 1983 (19830223)
JOURNAL: Section: E, Section Number 288, Volume 09, Number 4, Pg. 167, January 10, 1985 (19850110)

ABSTRACT

PURPOSE: To increase tensile strength, to reduce cost and to eliminate the need for a corrosion-resisting and acid-resisting protection by plating the surface of a superfine core wire made of a **conductive** metal with gold.

CONSTITUTION: The core wire 1 of a wire for bonding a semiconductor element is made of a **copper** alloy containing **copper** or tin. A gold plating layer 2 is applied on the surface of the core wire 1 through an **electroplating** method or a hot dipping method. Oxygen-free **copper** of not less than 99.99% purity is used as **copper** in the core wire 1. The **diameter** of the core wire 1 is approximately 0.02mm, and the thickness of the layer 2 is approximately 0.0025mm. 10-15% of the **diameter** of the core wire 1 is

preferable as the thickness of the layer 2. The whole is annealed as required. The breaking strength (A) of the wire not annealed is higher than that (C) of conventional gold wires within a total temperature range, and the breaking strength (B) of the wire annealed is higher at approximately 200c or more. With the wire annealed, a bending is small and linearity is excellent on a winding or a rewinding to a bobbin, and a large solid loop can be obtained.

61/3,AB/12 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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01331962
MANUFACTURE OF THICK FILM HYBRID IC

PUB. NO.: 59-043562 [JP 59043562 A]
PUBLISHED: March 10, 1984 (19840310)
INVENTOR(s): RIKITAKE KYOICHI
KOYAMA MASATAKA
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 57-153966 [JP 82153966]
FILED: September 06, 1982 (19820906)
JOURNAL: Section: E, Section Number 251, Volume 08, Number 131, Pg. 146, June
19, 1984 (19840619)

ABSTRACT

PURPOSE: To obtain a thick hybrid IC which has high reliability by using as an insulating layer a heat resistance silicone resin, devising the manufacturing steps, thereby enabling to form a thick film resistance element by high temperature annealing on a metal substrate.

CONSTITUTION: An insulating layer and a heat resistance silicone resin 2 which is used as an adhesive are coated on a metal substrate 1 which is made of alloy of **nickel** an iron, and a resistor 4 which is made of oxidized ruthenium by high temperature annealing. Then, epoxy resin adhesive 5 is printed, a **copper** foil 6 is bonded, and patterned by etching. Then, the resistor 4 and a steel foil pattern 6 are connected by **conductor** 7 which is made by **electroless plating** method, an IC chip 8 is mounted, and connected via a **wire** 9 to the **pattern** 6. The step of forming the resistor 4 is employed before bonding the foil 6, thereby enabling the high temperature annealing of the resistor 4, and an inexpensive **copper** foil can be used as a **conductor**.

64/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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7394907 INSPEC Abstract Number: B2002-11-2550F-009

Title: Significant reduction of wire sweep using Ni plating to realise ultra fine pitch wire bonding

Author(s): Terashima, S.; Yamamoto, Y.; Uno, T.; Tatsumi, K.

Author Affiliation: Adv. Technol. Res. Labs., Nippon Steel Corp., Chiba, Japan

Conference Title: 52nd Electronic Components and Technology Conference 2002. (Cat. No.02CH37345) p.891-6

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2002 Country of Publication: USA xxxiv+1789 pp.

ISBN: 0 7803 7430 4 Material Identity Number: XX-2002-01381

U.S. Copyright Clearance Center Code: 0-7803-7430-4/02/\$17.00

Conference Title: Proceedings of 52nd Electronic Components and Technology Conference

Conference Sponsor: IEEE Components, Packaging, & Manufacture Technol. Society; Electronic Components, Assemblies & Mater. Assoc

Conference Date: 28-31 May 2002 Conference Location: San Diego, CA, USA

Language: English

Abstract: Significant reduction of the wire sweep in molding is proposed because the wire sweep is considered to be the major problem to realise wire bonding with ultra fine pitches of under 30 micrometers. In the present proposal, Ni was plated for several micrometers before molding on bonded Au wires. 'Ni plating' was carried out by means of **electroless plating** for several minutes in the aqueous solution kept at 358 K containing Ni and P. The wire sweep ratio for Ni plated wire (total diameter was 21 micrometers) was almost half of that for Au wire with the diameter of 15 micrometers except Ni plate, and was slightly smaller than that for Au wire with the diameter of 25 micrometers except Ni plate even the total diameter was smaller. It is considered that wire sweep suppression by this technique was due to the enhancement of both elastic and plastic properties.

Subfile: B

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64/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
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7341267 INSPEC Abstract Number: B2002-09-2240-007

Title: Mechanical properties of electroless Ni/Au wire bonded to an Al pad with the effects of chemical activation

Author(s): Woo-Jin Lee

Author Affiliation: Adv. Process Dept. 4, Hynix Semicond. Inc., Kyunggi, South Korea

Journal: Thin Solid Films vol.408, no.1-2 p.176-82

Publisher: Elsevier,

Publication Date: 3 April 2002 Country of Publication: Switzerland

CODEN: THSFAP ISSN: 0040-6090

SICI: 0040-6090(20020403)408:1/2L176:MPEW;1-3

Material Identity Number: T070-2002-009

U.S. Copyright Clearance Center Code: 0040-6090/02/\$22.00

Language: English

Abstract: The mechanical properties of electroless nickel (EN)

deposited onto pure gold (Au) wire used for the semiconductor industry have been investigated with the effects of the chemical activation, using the electrochemical quartz crystal microbalance (EQCM) technique, tensile, torsion and ball shear (BS) tests, and optical microscopy (OM). The combined results of in situ electrogravimetric curves with ex situ cross-sectional views obtained from the EN/Au **composite wire** clearly showed that EN deposits with the presence of pre-immersion Au were more rapidly formed on Au wire compared to the absence of the preimmersion Au. This is presumably due to the surface roughness increased by the hydrogen evolution as validated from OM. The load-displacement curves for the pre-immersion Au-coated and uncoated Au wires prior to EN revealed that the elastic modulus value of the EN outer layer, $E_{\text{sub Ni}}$, calculated on the basis of a linear elastic deformation model, was higher for the former than the latter. Moreover, it was found from the torsion and BS tests that the shear modulus of the EN, $G_{\text{sub Ni}}$, and the shear strength of the **composite wire** bonded to the aluminum (Al) pad with the zincate pretreatment were greater than for wires without this pretreatment; the values increased with increasing zincate immersion time. Consequently, it can be stated that the tensile strength of the EN/Au **composite wire** and the bonding strength between the wire and the Al pad are effectively increased by the existence of the pre-immersion Au layer and the zincate pretreatment, respectively.

Subfile: B

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64/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC
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7113554 INSPEC Abstract Number: B2002-01-1350H-052

Title: Demonstration of integral passives on double sided polyimide flex
Author(s): Nielsen, M.C.; Cole, H.S.; Saia, R.J.; Durocher, K.M.; Krishnamurthy, N.; Kapadia, H.; Lu, T.-M.; Rymaszewski, E.J.; Dey, S.; Shaefer, T.; Gilbert, B.

Author Affiliation: Gen. Electric Corp. Res. & Dev., Niskayuna, NY, USA

Conference Title: Proceedings 2000 HD International Conference on High-Density Interconnect and Systems Packaging (SPIE Vol.4217) p.351-6

Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA

Publication Date: 2000 Country of Publication: USA xvi+617 pp.

ISBN: 0 930815 60 2 Material Identity Number: XX-2001-01667

Conference Title: 2000 HD International Conference on High-Density Interconnect and Systems Packaging

Conference Sponsor: SPIE; IMAPS - Int. Microelectron. & Packaging Society; CMP Media

Conference Date: 25-28 April 2000 Conference Location: Denver, CO, USA

Language: English

Abstract: Understanding that integral passives can offer significant performance and cost leverages, the General Electric Research and Development Center, Schenectady, NY, has teamed with Rensselaer Polytechnic Institute (RPI), Arizona State University (ASU), Sheldahl, and the Mayo Foundation on the development of thin film deposition processes for the fabrication of passive elements on polyimide films. This program was targeted at developing manufacturing processes for the fabrication of integral resistors, capacitors and inductors to be used in digital and mixed mode (combined analog/digital) applications operating in the GHz regime. To demonstrate the developed technology, multichip modules were fabricated that included a microwave frequency downconverter circuit (shifting the input signal from 5 GHz to 500 MHz), a biphasic demodulator, a 500 MHz filter, a 5 GHz filter, and a splitter. The design and fabrication

methodology implemented a novel double sided flex approach, positioning the thin film capacitors on one side and the resistors and inductors on the reverse side. The capacitor material set consisted of tantalum oxide (Ta/sub 2/O/sub 5/) and diamond like carbon (DLC). **Spiral** geometric patterns of electroplated Cu formed the inductors, while the resistors used reactively sputtered tantalum nitride (Ta/sub 2/N). The high yield (>95%) of integral passive components on the fully functional multichip modules demonstrate the feasibility of incorporating thin film passive components with the manufacture of polyimide flex circuitry.

Subfile: B

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64/3,AB/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

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6874432 INSPEC Abstract Number: B2001-04-2550F-039

Title: Improvement of thermal stability of via resistance in dual damascene **copper** interconnection

Author(s): Oshima, T.; Tamaru, T.; Ohmori, K.; Aoki, H.; Ashihara, H.; Saito, T.; Yamaguchi, H.; Miyauchi, M.; Torii, K.; Murata, J.; Satoh, A.; Miyazaki, H.; Hinode, K.

Author Affiliation: Device Dev. Center, Hitachi Ltd., Tokyo, Japan

Conference Title: International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) p.123-6

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2000 Country of Publication: USA 871 pp.

ISBN: 0 7803 6438 4 Material Identity Number: XX-2001-00191

U.S. Copyright Clearance Center Code: 0 7803 6438 4/2000/\$10.00

Conference Title: International Electron Devices Meeting. Technical Digest. IEDM

Conference Sponsor: Electron Devices Society IEEE

Conference Date: 10-13 Dec. 2000 Conference Location: San Francisco, CA, USA

Language: English

Abstract: Thermal stability of via resistance in the multilevel dual damascene **Cu** interconnection was investigated. The via resistance stability strongly depends on via size, via density and width of connecting **Cu** wires. The significant via-resistance shift was introduced by stress-induced voiding. To avoid the voiding failure, optimization of heat treatments after **electroplating** (EP)-**Cu** deposition are necessary for both stability of **Cu** films and adhesion of barrier layer with **Cu**. Thermal stress balance between **Cu** wires and inter-level-dielectric (ILD) is also important to suppress the via degradation. The dual damascene structure with lower-stress and lower-Young's modulus ILD films such as FSG can provide wider process windows for the stability of the via resistance.

Subfile: B

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64/3,AB/5 (Item 5 from file: 2)

DIALOG(R)File 2:INSPEC

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6812088 INSPEC Abstract Number: B2001-02-2140-005

Title: Development of a new hybrid technology for inductive device applications

Author(s): Belloy, E.; Dezuari, O.; Gilbert, S.E.; Gijs, M.A.M.

Author Affiliation: Inst. of Microsyst., Swiss Fed. Inst. of Technol.,
Lausanne, Switzerland

Conference Title: 8th European Conference on Power Electronics and
Applications. EPE'99 p.6 pp.

Publisher: EPE Assoc, Brussels, Belgium

Publication Date: 1999 Country of Publication: Belgium CD-ROM pp.

Material Identity Number: XX-1999-00856

Conference Title: Proceedings of 8th European Conference on Power
Electronics and Applications. EPE 99

Conference Sponsor: Eur. Power Electron. & Drives Assoc

Conference Date: 7-9 Sept. 1999 Conference Location: Lausanne,
Switzerland

Language: English

Abstract: The authors describe the fabrication and characterisation of
2-dimensional inductive devices **integrated** inside printed
circuit boards (PCB) and flex-foils. Their devices basically are
composed of three layers of which the outer layers bear the printed
coil patterns and the inner layer is a high permeability
ferromagnetic sheet core. Both magnetic metal and **copper** layers are
patterned using standard lithographic techniques. **Electroplated**
interconnects between the outer layers complete the windings. They have
fabricated both transformers and fluxgate magnetic field sensing devices
with a thickness of 200 μm for the flex-foil devices and 600 μm for the
PCB-based devices. Lateral dimensions are approximately 1 cm. They realise
a magnetic field detection limit of 43 μT at 20 kHz for the fluxgate
devices relatively and inductances of 1-10 μH at a frequency of 1 kHz for
the transformers. Application of their devices is in magnetic field and
current sensing and in low power electronics, where miniaturisation is an
issue.

Subfile: B

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64/3,AB/6 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

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6465858 INSPEC Abstract Number: B2000-02-2210D-031

Title: Development of a novel printed circuit board technology for
inductive device applications

Author(s): Dezuari, O.; Gilbert, S.E.; Belloy, E.; Gijs, M.A.M.

Author Affiliation: Inst. of Microsyst., Swiss Fed. Inst. of Technol.,
Lausanne, Switzerland

Journal: Sensors and Actuators A (Physical) Conference Title: Sens.
Actuators A, Phys. (Switzerland) vol.A76, no.1-3 p.349-55

Publisher: Elsevier,

Publication Date: 30 Aug. 1999 Country of Publication: Switzerland

CODEN: SAAPEB ISSN: 0924-4247

SICI: 0924-4247(19990830)A76:1/3L.349:DNPC;1-F

Material Identity Number: N866-1999-013

U.S. Copyright Clearance Center Code: 0924-4247/99/\$20.00

Conference Title: Eurosensors Conference

Conference Date: 13-16 Sept. 1998 Conference Location: Southampton, UK

Language: English

Abstract: This paper describes the fabrication and characterisation of
2-dimensional inductive devices **integrated** inside printed
circuit boards (PCB) and flex-foils. These devices basically are
composed of three layers of which the outer layers bear the printed
coil patterns and the inner layer is a high permeability
ferromagnetic sheet core. Both magnetic metal and **copper** layers are

patterned using standard lithographic techniques. **Electroplated** interconnections between the outer layers complete the windings. We have fabricated both transformers and fluxgate magnetic field sensing devices with a thickness of 200 μm for the flex-foil devices and 600 μm for the PCB-based devices. Lateral dimensions are approximately 1 cm. We realise relatively high inductances of 1-10 μH at a frequency of 1 kHz for the transformers and a magnetic field detection limit of 43 μT at 20 kHz for the fluxgate devices.

Subfile: B

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64/3,AB/7 (Item 7 from file: 2)

DIALOG(R)File 2:INSPEC

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03613184 INSPEC Abstract Number: B90027918

Title: Plated **copper** on ceramic for power hybrid applications

Author(s): Weeks, R.; Johnson, R.W.; Hopkins, D.; Muir, J.; Williams, J.R.

Author Affiliation: Dept. of Electr. English, Auburn University, AL, USA

Conference Title: 1989 Proceedings. 39th Electronic Components Conference (Cat. No.89CH2775-5) p.544-50

Publisher: IEEE, New York, NY, USA

Publication Date: 1989 Country of Publication: USA xii+929 pp.

U.S. Copyright Clearance Center Code: 0569-5503/89/0544\$01.00

Conference Sponsor: IEEE; Electron. Ind. Assoc

Conference Date: 22-24 May 1989 Conference Location: Houston, TX, USA

Language: English.

Abstract: A technique for plating **copper** onto ceramic with top layers of **nickel**, gold, and/or solder is described. The adhesion mechanism of the **copper** is an interlocking of the film and ceramic surface to form a mechanical bond. Soldered adhesion of the **copper** did not degrade during high-temperature storage or thermal cycling. A **nickel** barrier between the plated **copper** and solder inhibits diffusion and intermetallic formation. Testing of small-diameter gold and large-diameter aluminum wire bonds after high-temperature storage demonstrated the reliability of wire bonding to the Cu/Ni /Au metallization. While a small percentage of bond lifts occurred among the aluminum -wire-bond samples stored at 200 degrees C, the bond strengths were high and there was no increase in series bond resistance. Preliminary evaluation of a screen-printable polyimide encapsulant revealed pinholes in the cured film. Alternate polyimide formulations are being evaluated. A 2-MHz, 100-W DC-DC converter was fabricated to demonstrate the use of plated **copper** on ceramic substrate technology.

Subfile: B

64/3,AB/8 (Item 1 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

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06711458

E.I. No: EIP04068010652

Title: Silicon-based miniature sensor for electrical tomography

Author: York, Trevor; Sun, Liling; Gregory, Chris; Hatfield, John

Corporate Source: Department of Electrical Engineering UMIST, Manchester M60 1QD, United Kingdom

Conference Title: Selected Papers from Eurosensors XVI Prague, Czech

Republic

Conference Location: Prague, Czech Republic Conference Date:
20020915-20020918

E.I. Conference Number: 62196

Source: Sensors and Actuators, A: Physical v 110 n 1-3 Feb 1 2004. p
213-218

Publication Year: 2004

CODEN: SAAPEB ISSN: 0924-4247

Language: English

Abstract: The paper describes the fabrication of a novel miniature sensor for electrical tomography. The sensor comprises a number of **copper** electrodes that are fabricated around a small hole that is etched through a silicon wafer. **Copper** electrodes are **electroplated** to fill channels that are formed in thick photo-resist on top of the silicon wafer. Electrodes with a thickness of 60µm, surrounding a hole of diameter 300µm, have been realised. Initial measurements have been made using a commercial LCR meter applied to an eight-electrode sensor and images of a 80µm **diameter wire** have been obtained. Future work will consider the **integration** of measurement **circuitry** alongside the electrodes in order to reduce parasitic capacitances. copy 2003 Elsevier B.V. All rights reserved. 9 Refs.

64/3,AB/9 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online

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01632776 AAD9825366

A SINGLE **CHIP**, FULLY INTEGRATED, **TELEMETRY** POWERED SYSTEM FOR
PERIPHERAL NERVE STIMULATION (NEUROMUSCULAR STIMULATION)

Author: VON ARX, JEFFREY ALLEN

Degree: PH.D.

Year: 1998

Corporate Source/Institution: THE UNIVERSITY OF MICHIGAN (0127)

Source: VOLUME 59/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 807. 129 PAGES

This work describes the first telemetry powered implantable microsystem to be fully integrated onto a single **chip**. This system is an 8-channel programmable neuromuscular stimulator for use with peripheral nerve electrodes. This implant receives all power and data through inductive coupling with an integrated, on-**chip** coil. Therefore, it requires no batteries or transcutaneous leads. Because it is fully integrated, this is one of the smallest wireless implantable stimulators ever developed.

The system's stimulating output is a biphasic current waveform with a programmable interphase delay. Each phase has a 5-bit programmable amplitude of up to 2 mA, and a 10-bit programmable duration of up to 2 ms. The system is capable of stimulation frequencies of over 150 Hz. Full scale stimulation can be obtained through loads of up to 1.7 k Ω . The system is powered by a 4 MHz carrier, and data is sent by pulse width encoded amplitude modulation.

The system's **integrated circuitry** is Bi-CMOS, contains 3,100 transistors, and measures 2.0 mm by 8.7 mm. It includes an RF receiver, a 4 Volt DC supply generator, a 500 kHz clock generator, data detection circuitry, finite state machine controlled logic, a 5-bit DAC output current source, and low resistance output switches. This circuitry was fabricated, tested, and is fully functional. It consumes 14.8 mW from the 4 Volt supply during full scale 2 mA stimulation.

Integrated on-**chip** coils optimized for inductive powering were

developed as part of this work. These coils have **electroplated copper** windings, **electroplated** NiFe core, planar spiral design, and are CMOS compatible. Six different coil structures were fabricated, tested, and compared. A 2 by 10 mm, seventeen turn version of the best coil structure has an inductance of 2.9 μH and receives over 20 mW DC at a distance of up to 3 cm from a 8-cm **diameter** planar transmitter **coil**. An analytical model for inductive powering using on-chip coils has been developed, and the design of the on-chip coils was optimized using this model. General design guidelines for on-chip coils have been devised which, together with the analytical model, can be used to quickly implement on-chip coils for inductively powering many different microsystems.

64/3,AB/10 (Item 1 from file: 350)
 DIALOG(R)File 350:Derwent WPIX
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014552913

WPI Acc No: 2002-373616/200241

XRAM Acc No: C02-105808

XRPX Acc No: N02-292026

Polishing composition for e.g. substrates for semiconductors, photomasks, memory hard disks, comprises abrasive of preset particle size, chelating compound, protective layer formation compound, hydrogen peroxide and water

Patent Assignee: FUJIMI INC (FUJI-N); FUJIMI INC KK (FUJI-N)

Inventor: ASANO H; INA K; KITAMURA T; SAKAI K

Number of Countries: 031 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1182242	A1	20020227	EP 2001307117	A	20010821	200241 B
JP 2002075927	A	20020315	JP 2000253349	A	20000824	200241
US 20020043027	A1	20020418	US 2001928996	A	20010815	200241
CN 1340583	A	20020320	CN 2001122298	A	20010822	200246
KR 2002016596	A	20020304	KR 200151445	A	20010824	200258
US 6440186	B1	20020827	US 2001928996	A	20010815	200259
TW 539735	A	20030701	TW 2001120020	A	20010815	200379

Priority Applications (No Type Date): JP 2000253349 A 20000824

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
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EP 1182242	A1	E	15	C09G-001/02
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Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT

LI LT LU LV MC MK NL PT RO SE SI TR

JP 2002075927	A	8	H01L-021/304
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US 20020043027	A1		C09K-003/14
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CN 1340583	A		C09G-001/02
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KR 2002016596	A		C09K-003/14
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US 6440186	B1		C09G-001/02
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TW 539735	A		C09G-001/02
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Abstract (Basic): EP 1182242 A1

Abstract (Basic):

NOVELTY - Polishing composition comprises:

- (1) an abrasive of primary particle size of 50-120 nm;
- (2) a compound capable of forming a chelate with **copper** ions;
- (3) a compound to provide a protective layer-forming function to **copper** layer;
- (4) hydrogen peroxide; and
- (5) water

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a polishing method which involves polishing the semiconductor devices containing at least a layer of **copper** and tantalum compound formed on a substrate, using the polishing composition.

USE - For polishing substrates for semiconductors, photomasks, memory hard disks, particularly for planarization of the surface of device wafers in semiconductor industry.

ADVANTAGE - The polishing composition is highly efficient and forms an excellent polished surface on semiconductor devices. The abrasive has effective primary particle size and suppresses pits on the **copper** wiring. The carboxyl group and nitrogen atom located at the alpha position of the chelating compound forms a chelate with the **copper** thereby accelerates polishing of the **copper** layer. The compound with protective layer forming function, protects the **copper** layer during and/or after the polishing and consequently suppresses dishing or formation of recesses in the **copper** wiring and thus functions as a corrosion preventive agent to suppress the corrosion of **copper**. Hydrogen peroxide has sufficient oxidation power to oxidize the **copper** layer and contains low metal ion as impurity. The polishing method provides a high stock removal rate of the **copper** layer and a low stock removal rate of the titanium containing compound layer.

pp; 15 DwgNo 0/0

64/3,AB/11 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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008580648

WPI Acc No: 1991-084680/199112

XRAM Acc No: C91-036212

Zinc-nickel-alloy **electroplating** steel plate prodn. - by
polishing steel pre-plating and final plating, forming **chip**
-resistant material for cars

Patent Assignee: KAWASAKI STEEL CORP (KAWI)

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 3031496	A	19910212	JP 89166173	A	19890628	199112 B
JP 2790319	B2	19980827	JP 89166172	A	19890628	199839

Priority Applications (No Type Date): JP 89166172 A 19890628; JP 89166173 A 19890628

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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JP 3031496	A		7		
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JP 2790319	B2		5	C25D-005/26	Previous Publ. patent JP 3031496
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Abstract (Basic): JP 3031496 A

The method comprises (1) polishing a steel plate with a polishing material with abrasive grains; (2) pre-plating at the mol. ratio $Ni/(Zn+Ni) = 0.9-1$, pH 1-2, current density 5-150 A/dm², plating amount 50-1000 mg/m²; and (3) Zn-Ni-alloy-**electroplating**.

Pref. the grain size of the abrasive grains is 100-1000. The polishing material is a brush-roller with a brush wire diameter of less than 1.6mm.

USE/ADVANTAGE - The Zn-Ni-alloy-**electroplated** steel plate is useful as outside plate of cars. It has good

chipping-resistance, corrosion-resistance and coating property, with a small number of coatings. (7pp Dwg.No.0/0)

64/3,AB/12 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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003214970

WPI Acc No: 1981-75526D/198141
Fine bore formed by **electroforming** core wire - of identical dia. to produce electro-cast rod which is sliced prior to wire removal

Patent Assignee: RICOH KK (RICO)

Inventor: HAGA H; IKEDA K

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4290857	A	19810922				198141 B
JP 55158984	A	19801210				199103

Priority Applications (No Type Date): JP 7967067 A 19790530

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4290857	A		7		

Abstract (Basic): US 4290857 A

A fine bore ink head is produced by electro-forming a core line having the same dia. as that of the fine bore to be formed to form an electro-formed layer around the **core wire**. The **composite** electro-formed rod is sliced into disc-shaped **chips** contg. the core wire and the wire is removed by dissolution or heating to form a fine bore of the same dia. as the core wire. Mfr. of a head for an ink jet plotter.

The fine bore is easily formed with a good cylindrical shape and has high wear resistance when used for liq. injection. A **Cu** wire (1) is electro-formed to produce an electro-forming layer (2) around the **wire** and form a **composite** rod having an electrocast layer (2) of **Ni** around the **Cu** wire. The rod is sliced into disc shapes (7) approx. 0.20 mm thick and a spherical recess (5) is formed by grinding one surface of each **chip**. Each **chip** is placed in a 10% NaCN soln. so as to dissolve and remove the core wire to leave a fine bore having a dia. identical to that of the core wire.

6

64/3,AB/13 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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06185402

HYBRID INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE

PUB. NO.: 11-126952 [JP 11126952 A]

PUBLISHED: May 11, 1999 (19990511)

INVENTOR(s): IGARASHI YUUSUKE
SAKAI NORIHIRO
NAKAMURA TAKESHI
KANAZAWA KATSUHIRO
KOBAYASHI YOSHIYUKI

APPLICANT(s): SANYO ELECTRIC CO LTD

APPL. NO.: 09-289875 [JP 97289875]
FILED: October 22, 1997 (19971022)

ABSTRACT

PROBLEM TO BE SOLVED: To eliminate the need for heating the circuit board of a hybrid **integrated circuit** by omitting Au thin wires and Au coatings by coating a first electrode on the circuit board side and a second electrode on a flexible sheet side with **Ni** and connecting metallic wires composed of the coating **Ni** and **Al** to each other by **wire bonding**.

SOLUTION: **Cu patterns** 14, 18, and 20 are formed on the circuit board 11 of a hybrid **integrated circuit** insulated with an insulating material 12. Then the surface of the circuit board 11 is coated with a resist film 41 having a rectangular window 40 and **electroplating** is performed. After **electroplating**, **Ni** coatings 42 are formed on pads 20 by impressing voltages upon wires 18 so as to make electric currents flow. In addition, a flexible sheet is stuck to the board 11 with an adhesive. Finally, **Al** thin wires are bonded after the adhesive is cured. Therefore, the wire bonding of the **Al** thin wires becomes possible at a room temperature and the bondability of the thin wires can be improved, because the flexible sheet itself can prevent the softening of the underlying adhesive.

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64/3,AB/14 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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01391721
MANUFACTURE OF COIL

PUB. NO.: 59-103321 [JP 59103321 A]
PUBLISHED: June 14, 1984 (19840614)
INVENTOR(s): KANO OSAMU
MAKITA TAKASHI
SENDA ATSUO
APPLICANT(s): MURATA MFG CO LTD [000623] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-212989 [JP 82212989]
FILED: December 03, 1982 (19821203)
JOURNAL: Section: E, Section No. 270, Vol. 08, No. 217, Pg. 155,
October 04, 1984 (19841004)

ABSTRACT

PURPOSE: To effectively obtain a **chip** type coil by opposingly forming slender through slits to an **insulating** substrate with the specified interval, depositing metal layer to the front and rear surfaces of substrate and internal wall of slits, thereafter removing metal layer leaving that at the coil lead forming area and by cutting the substrate along the slits.

CONSTITUTION: A plurality of slender through slits 11 are formed in parallel with the specified interval to an insulating substrate 10 consisting of ceramic, plastic and glass and metal layer 12 such as **copper** is deposited to the front surface 14, rear surface 15 of substrate 10 and the internal surface 13 of slits 11 by the **electroless plating**, etc. In view of leaving only the metal layer 12 for connecting the internal surfaces 13 of slits, such part is

covered with the photo resist. Then, substrate is immersed into the ferric sulfate solution in order to remove the unwanted layer 12, leaving only the layer 12 which will become the **coil pattern** 16. Thereafter, the substrate 10 is cut along the slits 11 and a **coil** where the **pattern** 16 is formed at the front and rear sides through the internal surface 13 of slit at both ends can be obtained.

64/3,AB/15 (Item 3 from file: 347)

DIALOG(R)File 347:JAPIO

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00770695

FORMING METHOD FOR FINE PORE

PUB. NO.: 56-090995 [JP 56090995 A]

PUBLISHED: July 23, 1981 (19810723)

INVENTOR(s): UEISHI YUKIHIRO

IKEDA KUNIO

APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 54-167378 [JP 79167378]

FILED: December 21, 1979 (19791221)

JOURNAL: Section: C, Section No. 75, Vol. 05, No. 160, Pg. 114,
October 15, 1981 (19811015)

ABSTRACT

PURPOSE: To simply and precisely form the corrosion resistant fine pore on the inner circumferential face, by removing the wire rod leaving behind the corrosion resistant alloy layer formed by the wire rod and **electroforming** layer after forming the **electroforming** layer on the wire rod having the **wire diameter** nearly equal to desired diameter of the fine pore and carrying out heating diffusion treatment.

CONSTITUTION: The wire rod (for example; **copper wire**) 1 having desired **diameter** of fine pore, for example, a little larger than 30 μ , is prepared. Next, the **electroforming** rod 3 formed the **electroforming** layer 2 which is composed of Ni etc., is prepared on the circumference of the rod 1 by fixing the rod 1 on the jig for **electroforming** stretching rectilinearly and **electroforming**. Then, the spindle 4 is set centering the rod 1 of the rod 3 and carrying out the outer circumference processing by the gyratory cutting tool 5 and then, the rod 3 is finished up so as to be situated the rod 1 in the central point. Further, after finishing the concentric process, the rod 3 is sliced to **chip** 7 having a prescribed thickness by cutter bar 6. After that, the **chip** 7 is heated and corrosion resistant alloy layer consisting of the rod 1 and the layer 3, is formed. Next, the rod 1 is dissolved by warm solution of NaCN etc. and is removed leaving behind the alloy layer to form fine pores.